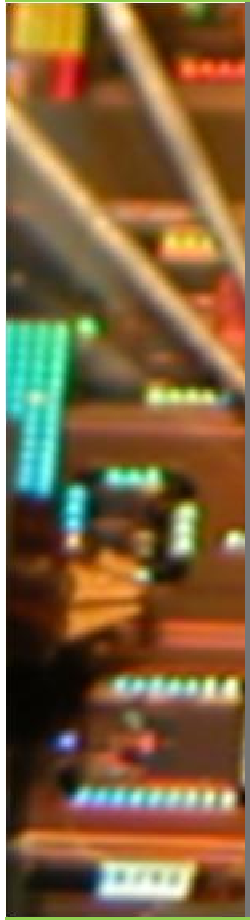


Battery-less wireless sensors based on low power UHF RFID tags

Battery-less wireless devices

Seville,
September 2010

Index

- Introduction
- Wireless sensor tag issues
- Passive tag design
- Implementation
- Results
- Conclusions

Introduction

Medical applications in the future are likely to benefit greatly from ultra low power electronics especially in implanted, home care, surgical, and emergency monitoring.

- Aging population.
- Increasing quality of life expectancy: new medical treatment trends
  - Monitoring.
  - Wireless.
  - Battery-less.
  - Home care.
- Rapid technology development.
- Increase asset utilization with real-time tracking.
- Reduce errors by tracking medical devices.

Introduction
RFID Sensor Healthcare Applications

- Medicine and Healthcare:
  - Fall Detection
  - Pressure sensor on medical instruments
  - Patient temperature
  - Parkinson
  - Post surgery awakening
  - Etc.

Introduction
Healthcare trends

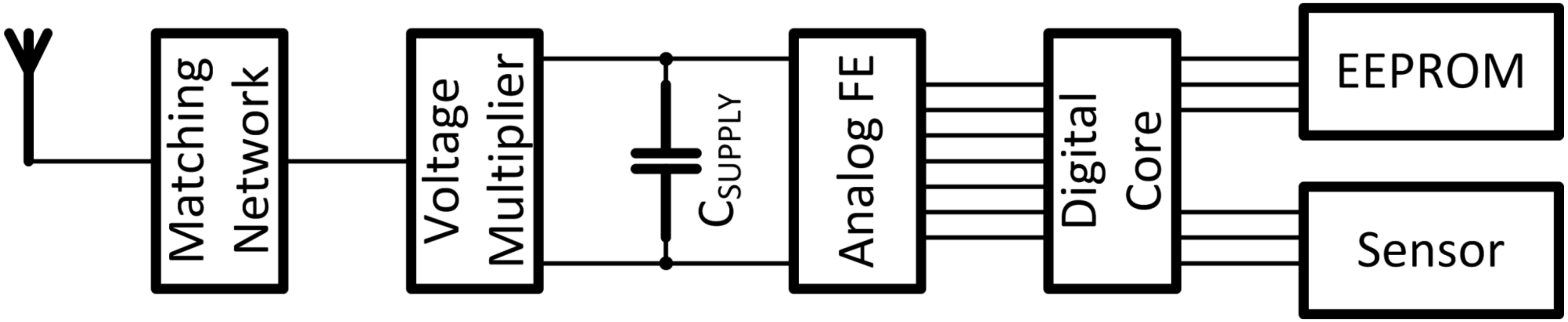
- Cost reduction can be achieved using home-based telemonitoring services.
  - Fewer days in hospitals.
- Home telemonitoring has also led to very high patient satisfaction.
- New motivation for the development of low-power noninvasive medical-monitoring devices: reduce health care costs.
- Power problem: the most critical limitation of previous realizations
  - Medical monitoring has been focused on reducing the overall power consumption of such devices.
  - Batteries must be removed: heavy, cost, constant recharging or replacing.
- To succeed this objective:
  - Low power rectifiers to harvest RF power in voltage and current capabilities to supply analog, processing and communication circuits, and the sensor.
  - Ultra-low-power sensors.

Wireless sensor tag issues

- Power is the main problem.
  - Active devices causes the main power dissipation when radio is active.
  - Reduce the standby power.
  - Minimize peak currents.
- Time, a problem related to power.
  - More transmission and/or acquisition imply more power consumption.
- Size, an important issue.
  - Antenna.
  - Passives and quartz required by the radio devices.
  - Increase level of integration.

Passive solutions implementation

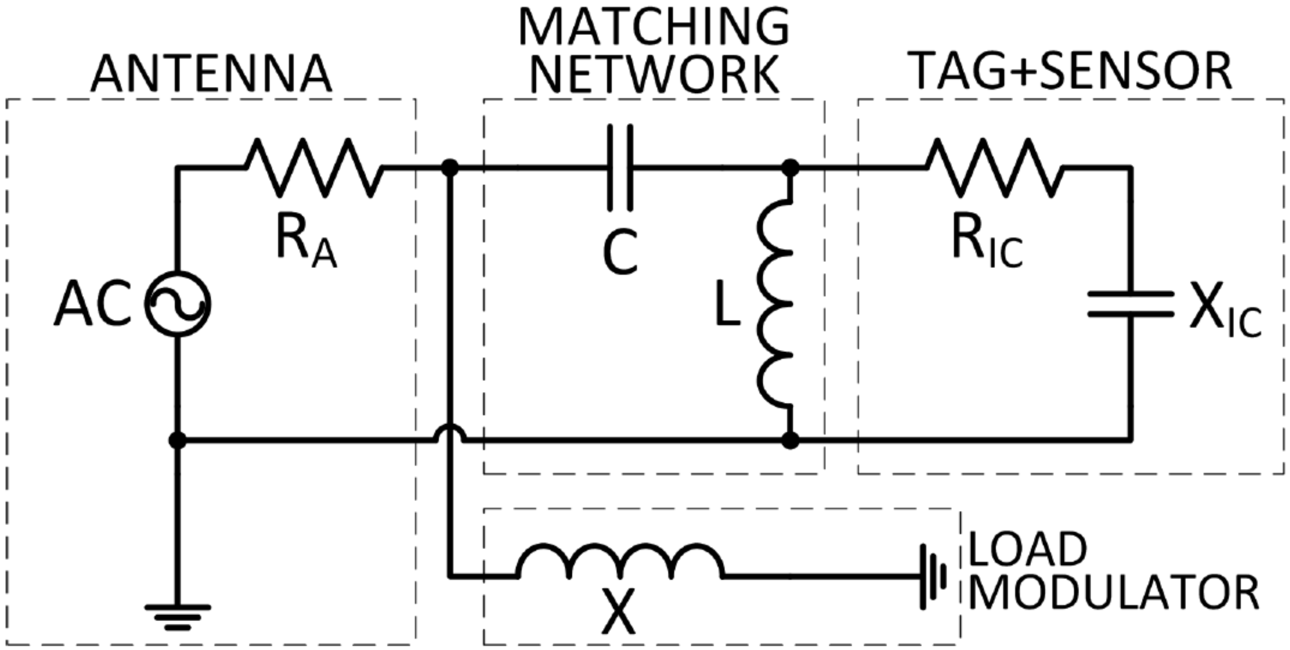
Passive tag design



- RF energy harvester: Voltage Multiplier (VM) and supply capacitor (C_{SUPPLY}).
- Band-gap and two voltage regulators.
- One unregulated output , in order to provide an input for external regulators.
- Voltage Limiter (VL)
- Clock generator.
- ASK demodulator.
- PSK Load modulator.
- Two Power-On-Reset (POR).
- Digital RFID UHF C1G2 protocol.
- Digital interface for sensor communication.

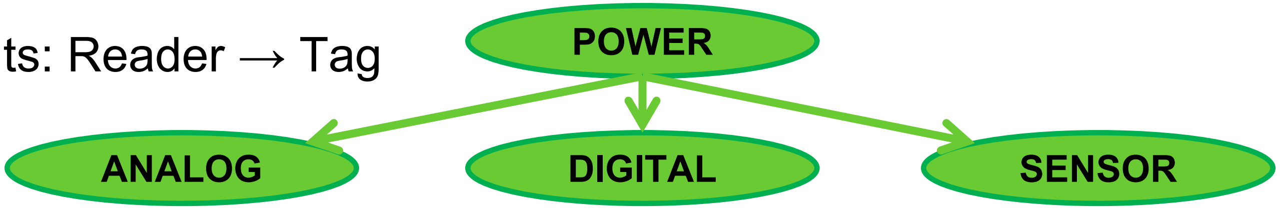
Passive tag design
System constraints

- Forward link constraints: Reader → Tag.
- Backward link constraints: Tag → Reader.

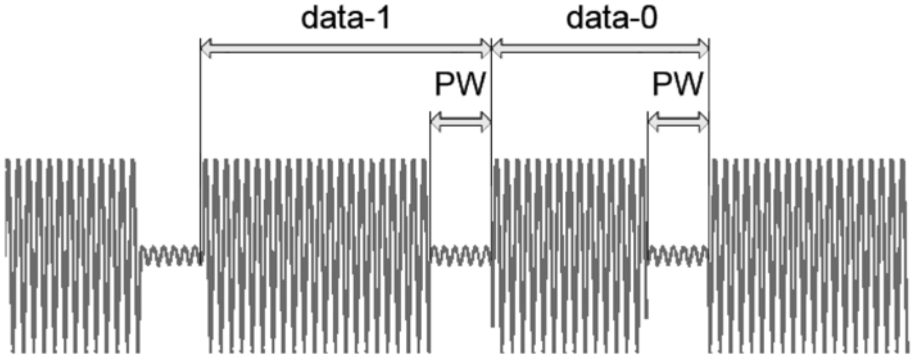


Passive tag design. System constraints
Forward link constraints: Reader → Tag (I)

- Forward link constraints: Reader → Tag
  - ➢Minimum input power.


POWER
ANALOG
DIGITAL
SENSOR

  - ➢Minimum voltage at the input of the voltage multiplier:
    - Input impedance.
    - FE quality factor.
  - ➢Modulation limitations
    - C_{SUPPLY} receives energy.
    - C_{SUPPLY} receives no energy.

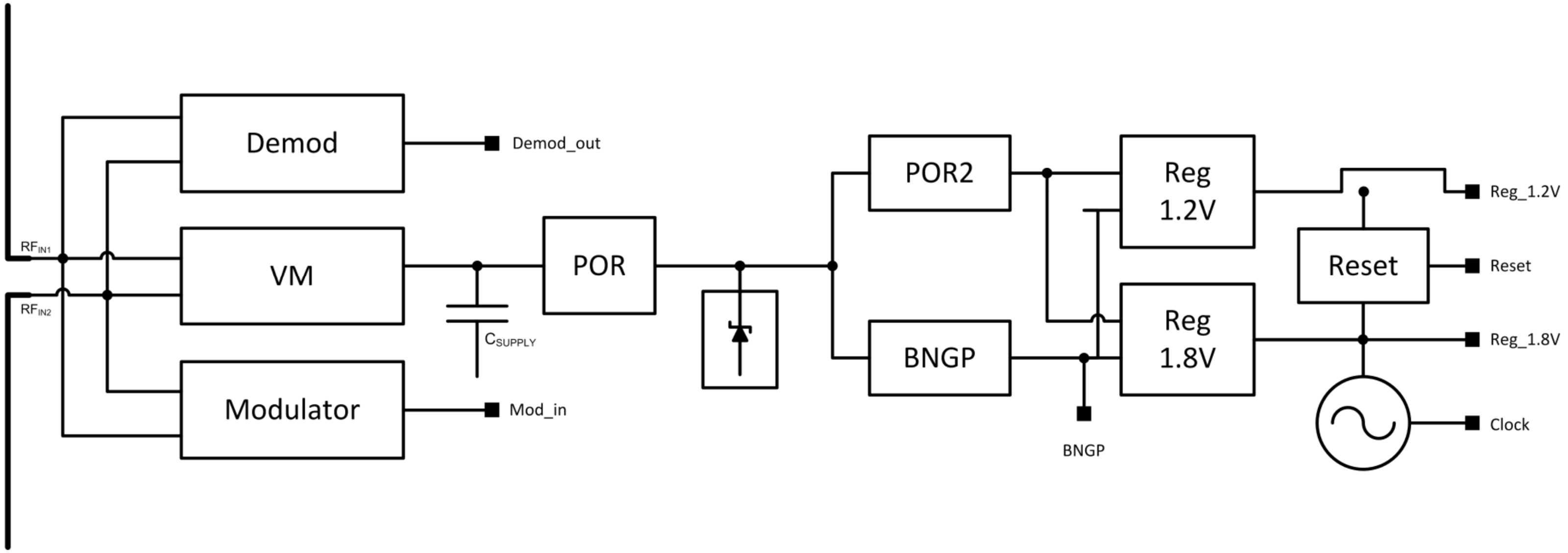


- Backward link constraints: Tag → Reader
  - ➢Probability error

$$P_{error} = \frac{1}{2}\left\{erf\left(\frac{Asin(\theta)(2cos(\varphi)-1)}{2\sigma}\right)erf\left(\frac{Asin(\theta)}{2\sigma}\right)\right\} \leq 10^{-3}$$

Passive tag design. Analog front-end

- Voltage Multiplier (VM) and supply capacitor (C_{SUPPLY}).
- Voltage Limiter (VL)
- Bandgap and two voltage regulators.
- Clock generator.
- ASK demodulator.
- PSK Load modulator.
- Two Power-On-Reset (POR).

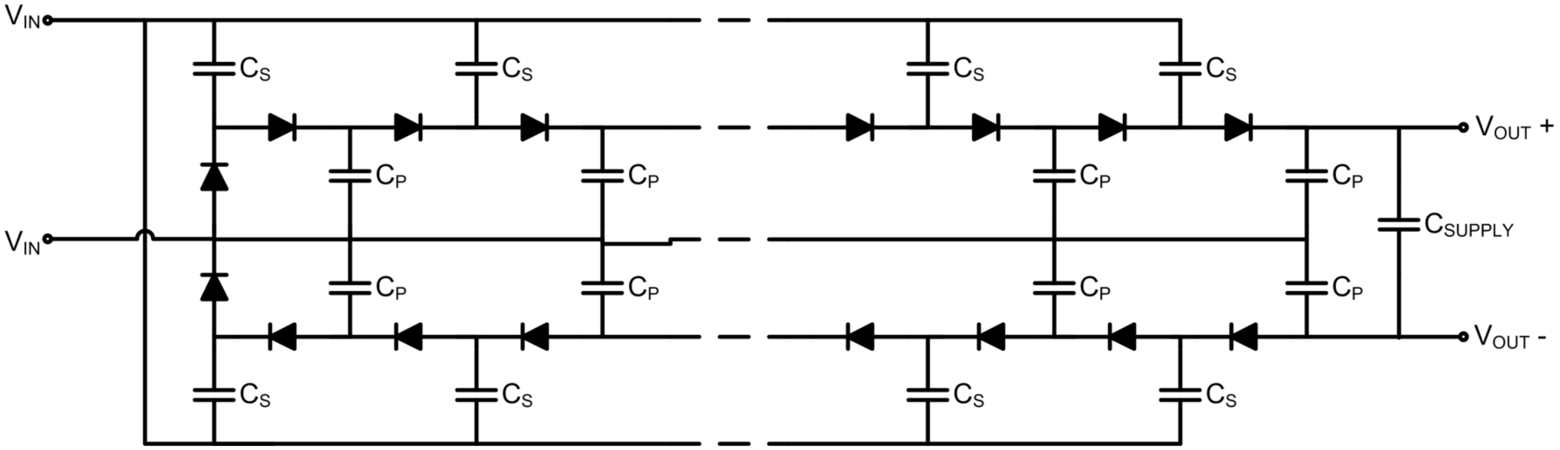


Simplified block diagram of the analog front-end.

Passive tag design. Analog front-end
Matching network and voltage multiplier (I)

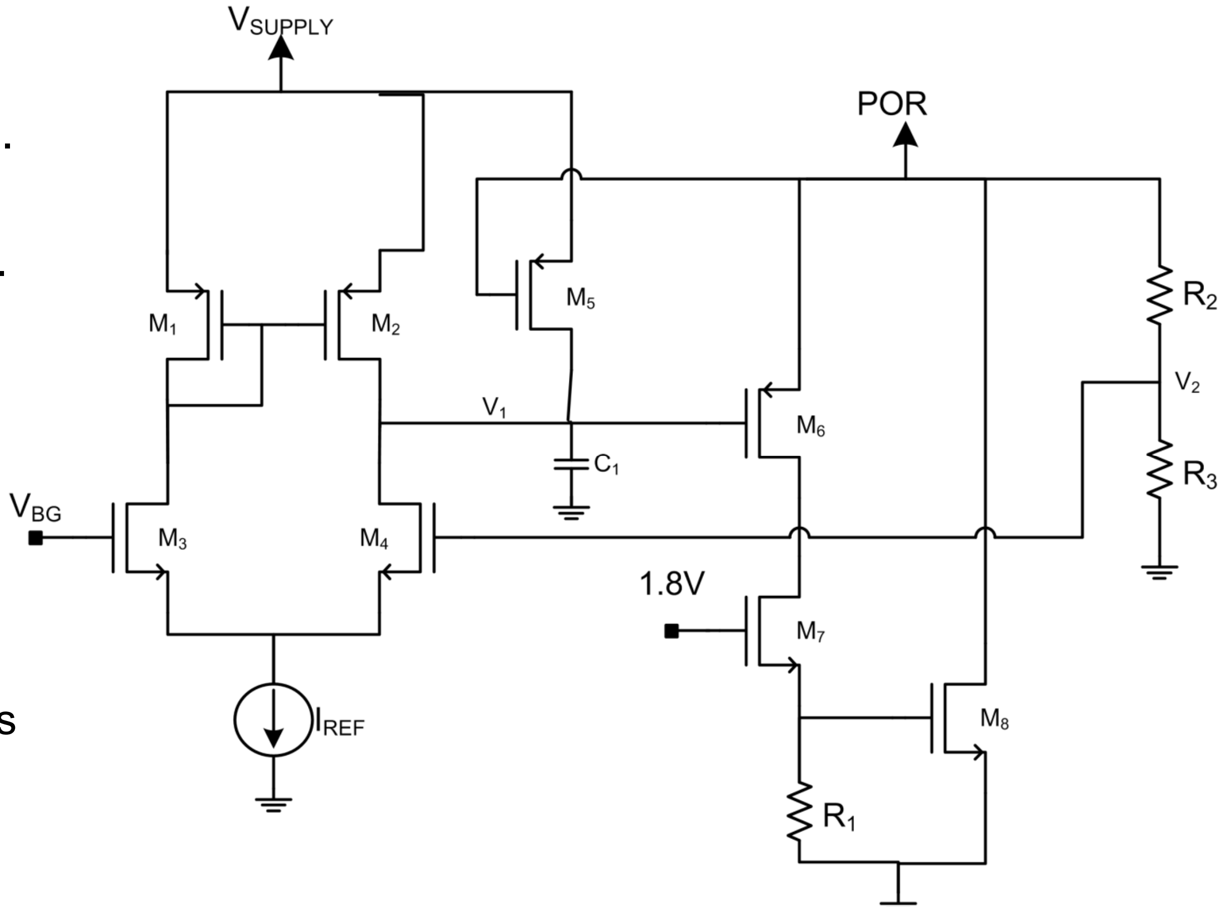
- Design steps: Q_{MN}, R_{IC}, N, diodes, C_S, C_P.
  - ➢ Determine the minimum input voltage (V_{MIN}) necessary for the correct performance of the tag without the matching network.
  - ➢ Calculate the input impedance.
  - ➢ Calculate the matching network to obtain the maximum power transference between the antenna and the tag.

N-stage Greinacher topology with the supply capacitor connected.



Passive tag design. Analog front-end
Voltage limiter

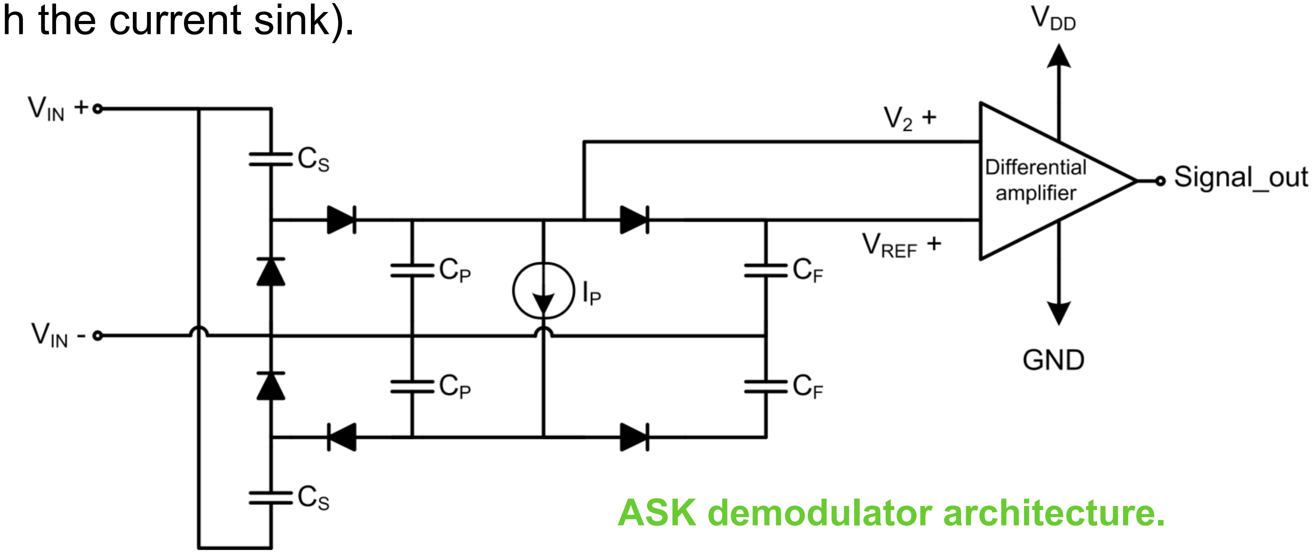
- Differential amplifier.
- Voltage supply ratio: V_2.
- V_2 and V_{BG} comparison.
- Limited value
  - very stable
  - V_{BG}, very stable against temperature and process variations.



Voltage limiter architecture.

Passive tag design. Analog front-end
ASK demodulator

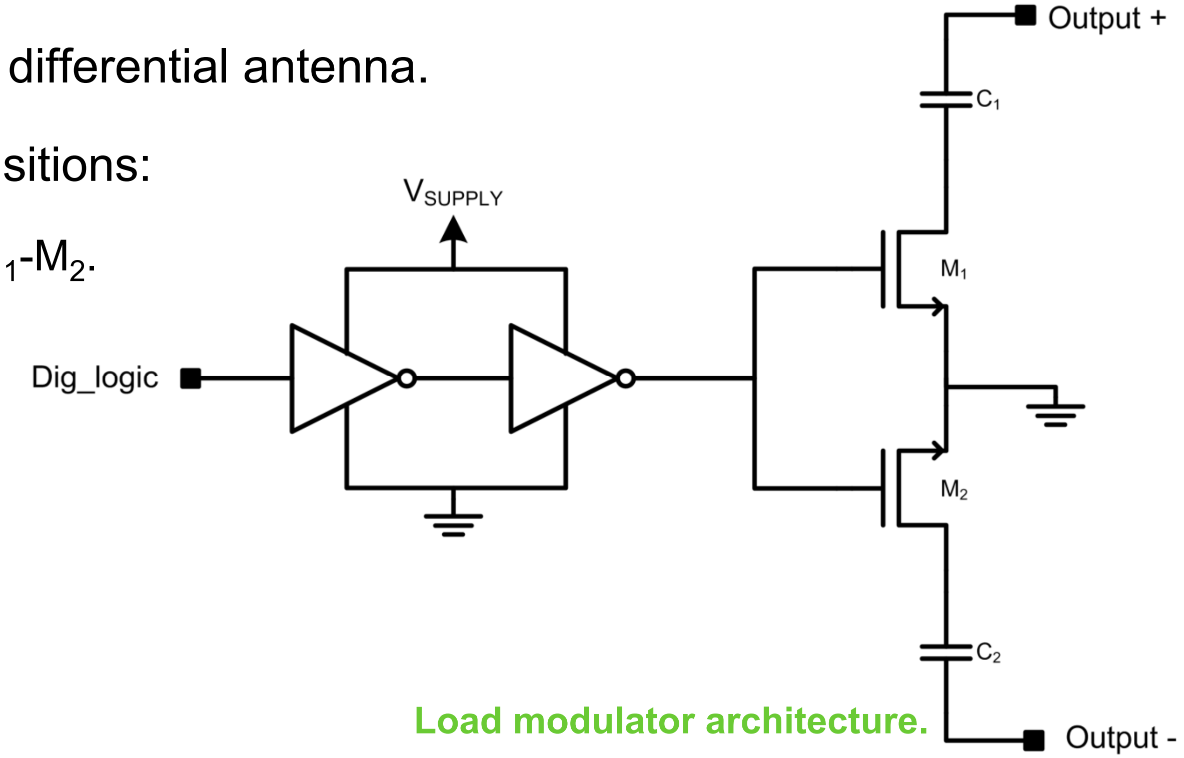
- Envelope detector: a rectifier in Greinacher's topology, a low-pass filter, implemented with diodes and capacitors C_F, and a differential amplifier.
- The incoming signal is modulated:
  - ➢ V_{REF+} remains constant (because diodes prevent C_F to discharge), while
  - ➢ V_{2+} discharges (through the current sink).
- ASK input impedance much higher than the VM input impedance.
  - ➢ Reduce the number of stages of the rectifier.



ASK demodulator architecture.

Passive tag design. Analog front-end
Load modulator

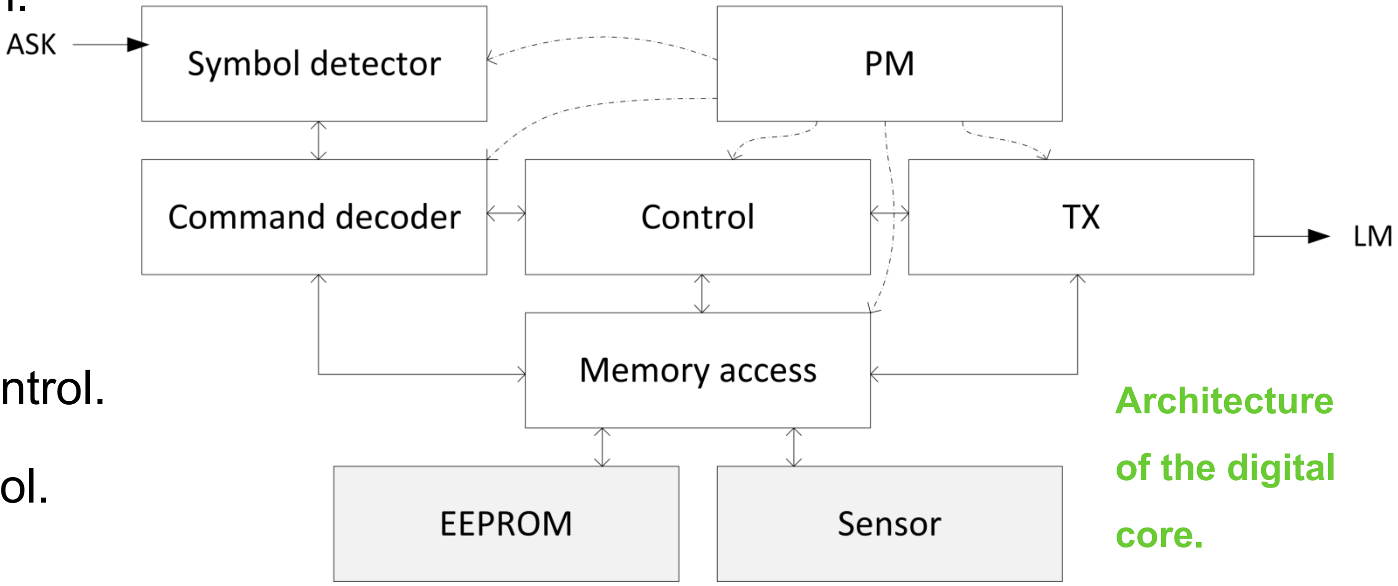
- Load modulator changes the input reactance of the tag:
  - PSK modulation is generated.
- Single switch and a capacitor.
- Output is connected to the differential antenna.
- Soft and spurious-free transitions:
  - High-input capacitance of M_1-M_2.
- Tag input impedance:
  - Reactance change.
    - Maximize phase difference.



Load modulator architecture.

Passive tag design. Digital core

- Logical intelligence to communicate with the reader making use of the analog front-end.
- The communication protocol defined in the standard has to be implemented on the design.
- EEPROM control.
- Sensor control.

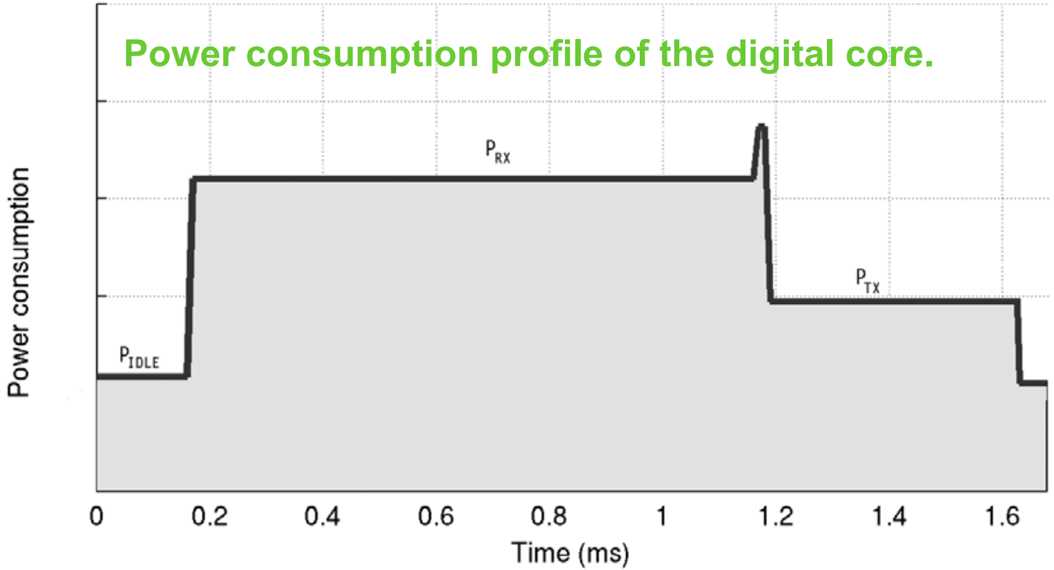


Architecture of the digital core.

Passive tag design. Digital core
Power management

Working states of the digital core.

	STRTP	STDBY	RX	CNTRL	TX
PM	ON	ON	ON	ON	ON
SYMBOL DETECTOR	OFF	ON	ON	OFF	OFF
COMMAND DECODER	OFF	OFF	ON	OFF	OFF
CONTROL	ON	OFF	OFF	ON	OFF
MEMORY ACCESS	ON	OFF	ON	ON	ON
TX	OFF	OFF	OFF	OFF	ON

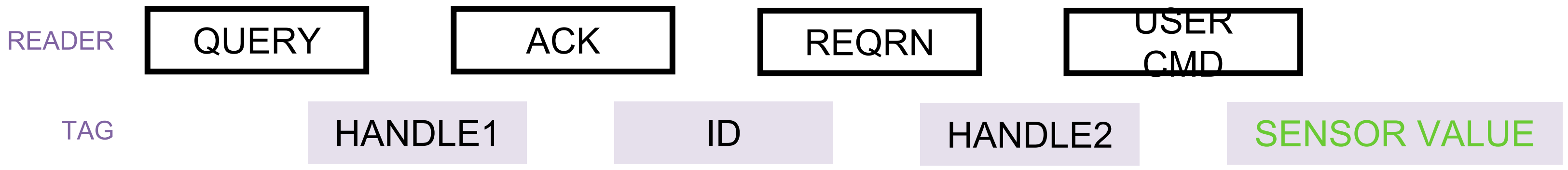

Power consumption profile of the digital core.

Passive tag design. Digital core
Sensor integration (I)

- The EPC C1G2 is specifically designed for identification applications and does not include support for sensors.
- Different approaches can be used to integrate sensors in C1G2 networks.
- In order to ensure the correct operation of the C1G2 network, compatibility between all the elements in the network is required.
- Three main approaches can be used:
  - Define a user command to access the sensor.
  - Replace part of the EPC with the measurement of the sensor.
  - Map part of the user memory bank to the sensor.

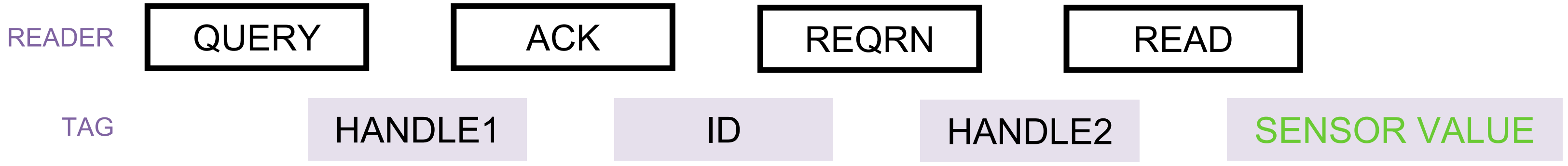
Passive tag design. Digital core
Sensor integration (II)

- User command.



- EPC substitution.

- Memory mapping.



Implementation

- Prototype of a wireless passive sensor combining:
  - Ultra-low power digital commercial sensor.
  - Module based digital core:
    - FPGA, its use makes the prototype to be versatile for any kind of sensor

    Power management.

    EPC C1G2 standard.

    Digital interface in order to communicate with the sensor.

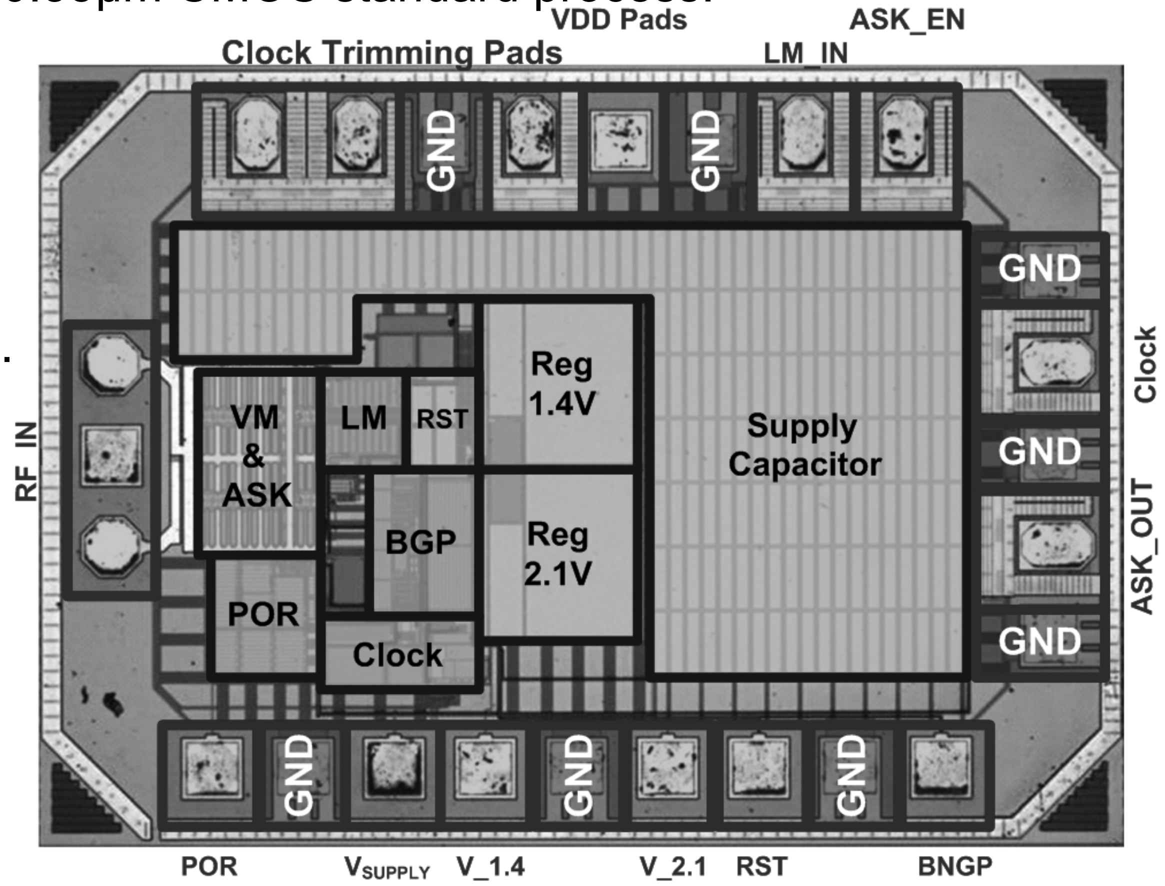
    - Digital core replica power consumption module.
  - Integrated analog frontend with three output voltages:
    - The analog front-end has been designed Two regulated at 1.4V and 2.1V.
    - One unregulated, but limited around 3.0V.
    - A low-drop out voltage regulator (LDO) is connected to 3.0V in order to supply many commercial sensors suitable for the desired prototype.

Implementation

- Analog front-end
- Digital core
- Digital commercial sensors
- Front-end setup with external regulator
- Prototype
  - Digital core power consumption
  - Supply capacitor
  - Sensor
  - Wireless sensor prototype
- Reader software implementation

Implementation
Analog front-end

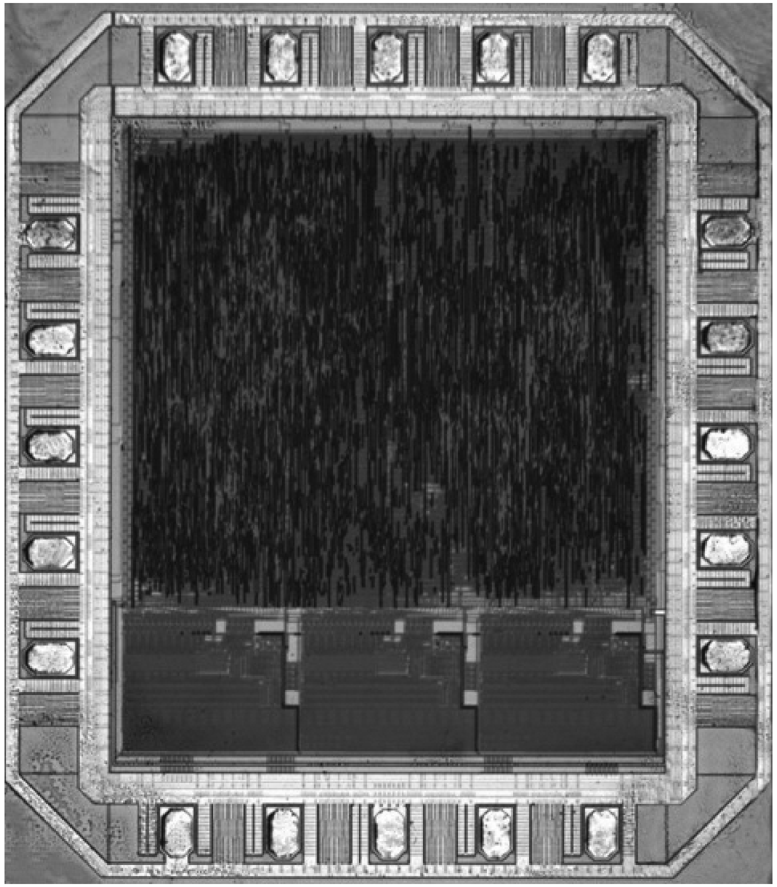
- A low cost 2-poly, 4-metal, 0.35μm CMOS standard process.
  - Schottky diodes.
  - High resistive poly.
  - EEPROM.
- 7.4μA current consumption.
- 1.4nF supply capacitor
  - area limitation.



RFID analog front-end layout (1777x1262μm^2).

Implementation
Digital core (I)

- The digital core design has been described in VHDL:
  - The design can be easily targeted either to ASIC or to FPGA implementation.
- A first version of the digital core has been implemented on ASIC for a 0.35µm process.
  - The design consists on an EPC C1G2 compatible core and a communication interface towards the sensor.
  - In the implemented version, a proprietary communication protocol has been used to communicate with a digital sensor



EPC C1G2 digital core layout.

Implementation
Digital core (II)

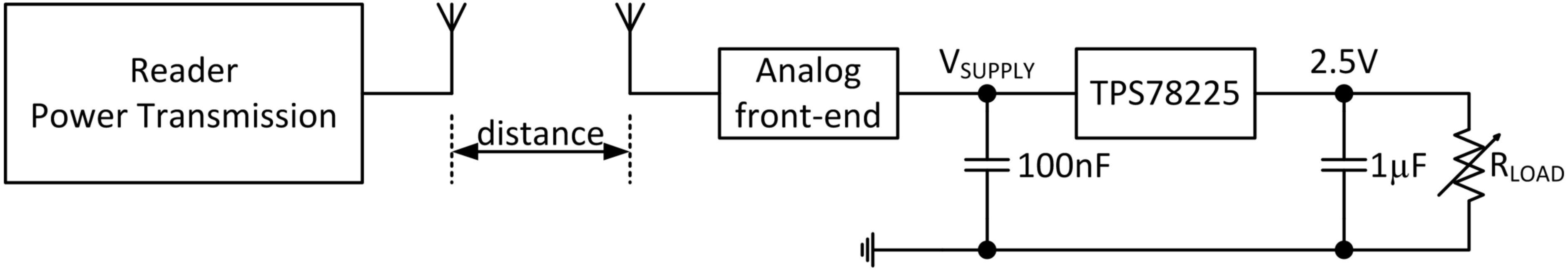
- In order to allow standard serial communication with commercial sensors, additional hardware is required.
- The implementation cannot be reused with a new sensor.
  - New physical hardware and pads are required.
- Solution to integrate a sensor in the tag allowing the communication with the digital core:
  - New code has been implemented in a FPGA.
  - The most common digital interface protocols have been added to the VHDL code of the digital core.
  - No need to fabricate the digital core for a fast and low cost prototype.

Implementation
Digital commercial sensors

- The current sensor market has a wide portfolio of low and ultra-low power devices.
- A complete range of commercial sensors offers accuracy and low cost with digital interfaces.
- Ultra-low power sensors:
  - ➢ low voltage operation: from 1.4V up to 5.5V.
  - ➢ low quiescent current: from 10μA up to 300μA.
  - ➢ Temperature, pressure, acceleration and humidity.
  - Sampling rate is directly correlated to the average power consumption.

Implementation
Front-end setup with external regulator

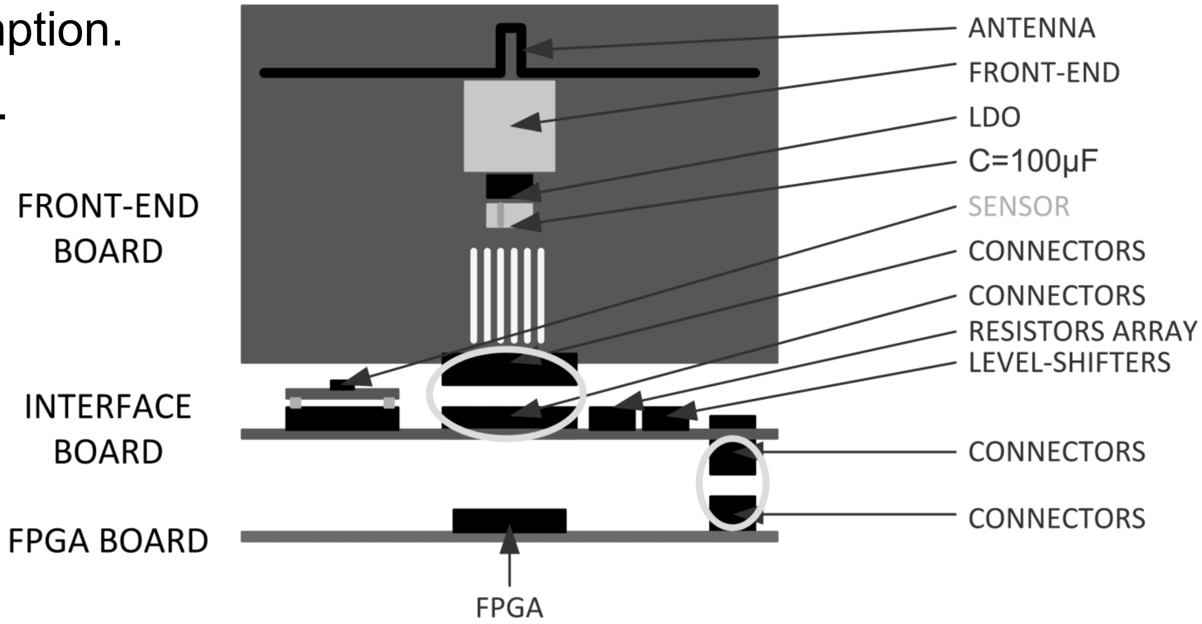
- Characterize the front-end capabilities to supply a sensor:
  - An ultra-low quiescent current LDO voltage regulator has been chosen.
  - TPS78225 from Texas Instruments, $I_Q = 1\mu A$.



- Reader emulated by a continuous wave 2W EIRP (European regulations).
- Dipole antenna for test purpose has been designed.
- LDO is connected between V_{SUPPLY} and a variable load (R_{LOAD}).
  - Measure the maximum current available for different distances.

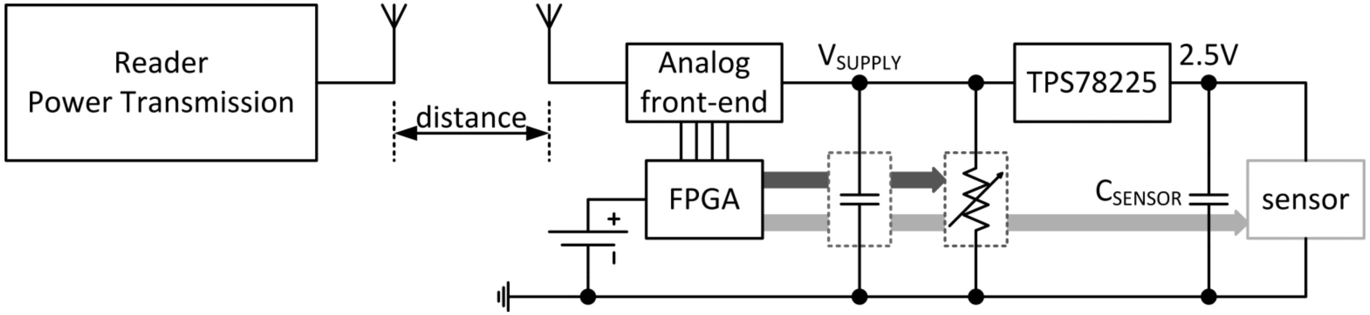
Implementation
Prototype

- Digital core power consumption.
- Wireless sensor prototype.
  - Front-end PCB.
  - FPGA PCB.
  - Interface PCB.

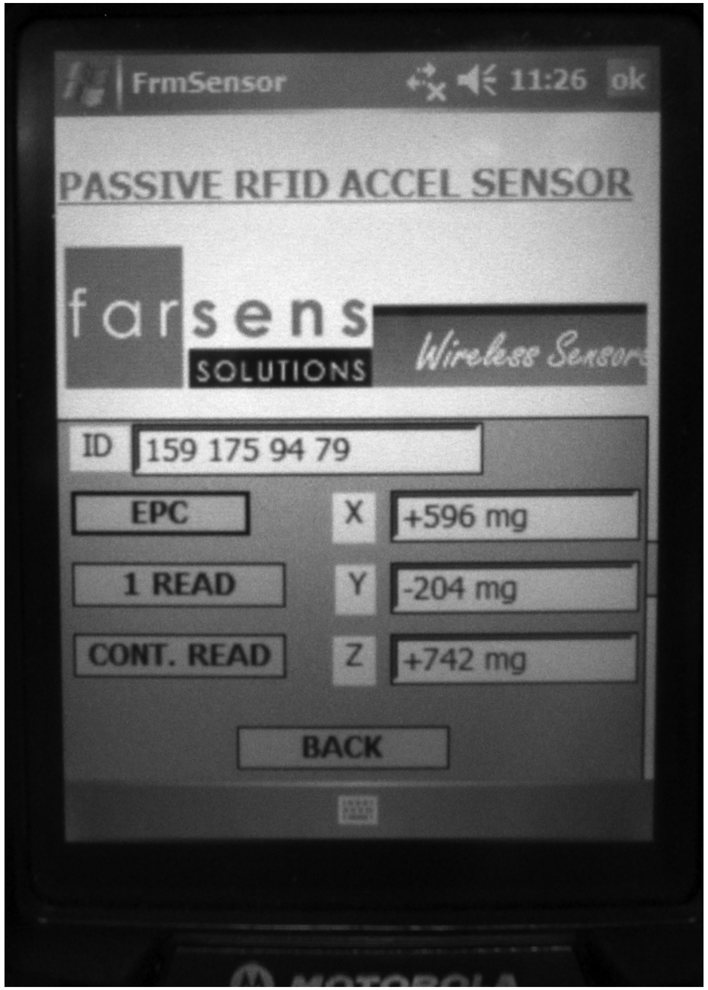


Implemented wireless sensor prototype scheme

Block diagram of the implemented prototype.



Implementation
Reader software implementation



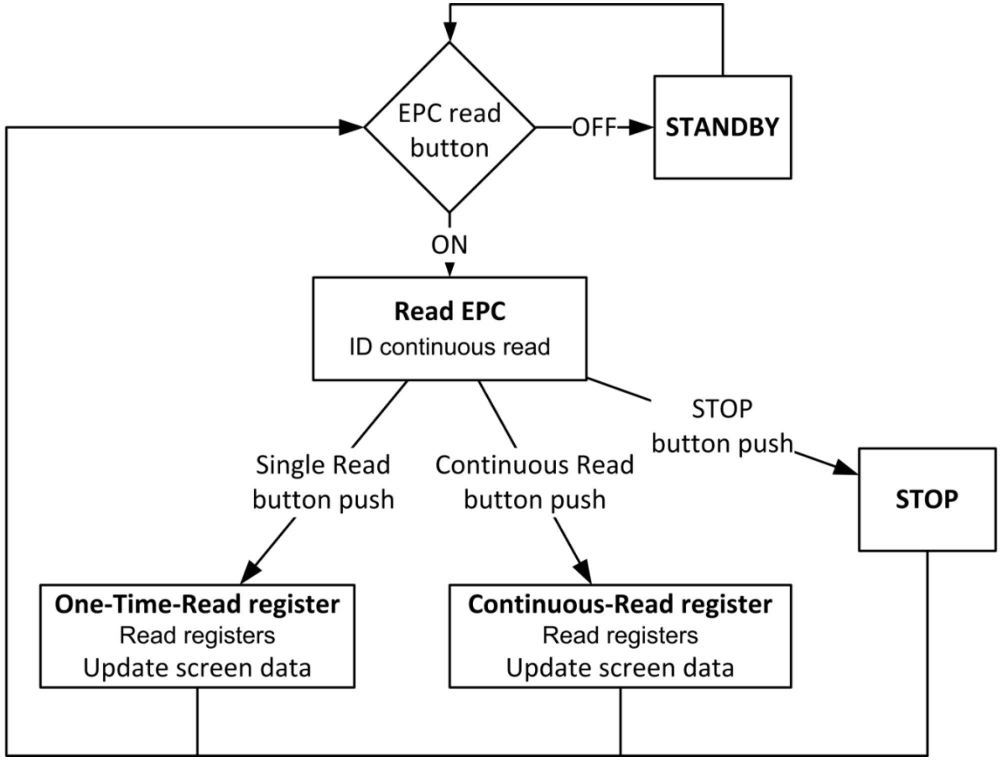
PASSIVE RFID ACCEL SENSOR

ID 159 175 94 79

X +596 mg

Y -204 mg

Z +742 mg



EPC read button

OFF

STANDBY

ON

Read EPC
ID continuous read

Single Read button push

Continuous Read button push

STOP button push

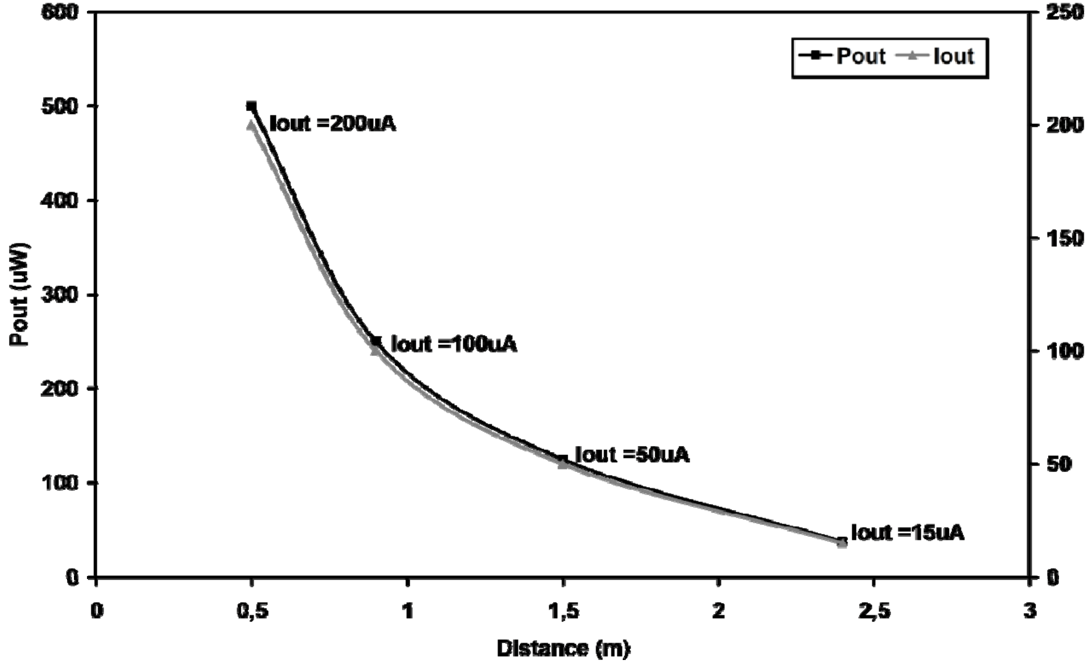
STOP

One-Time-Read register
Read registers
Update screen data

Continuous-Read register
Read registers
Update screen data

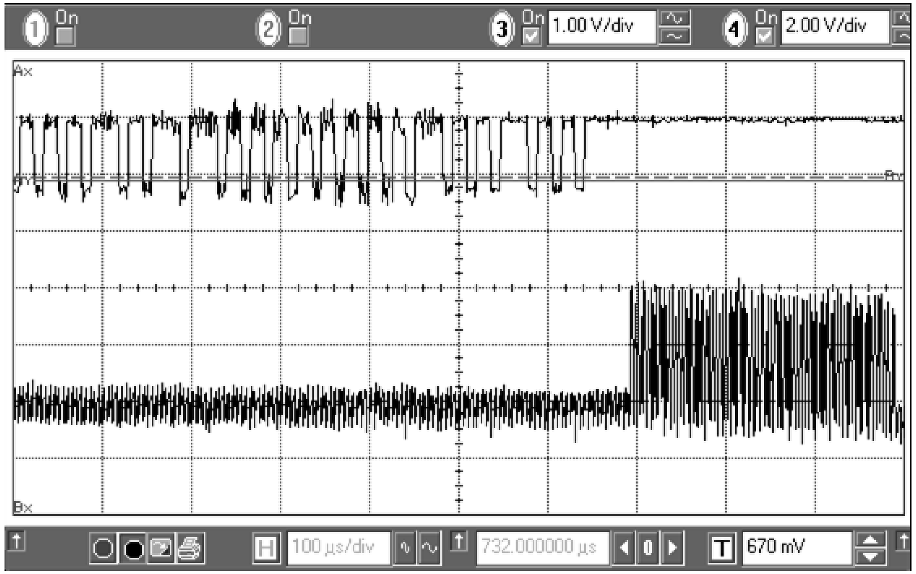
Results
Front-end results

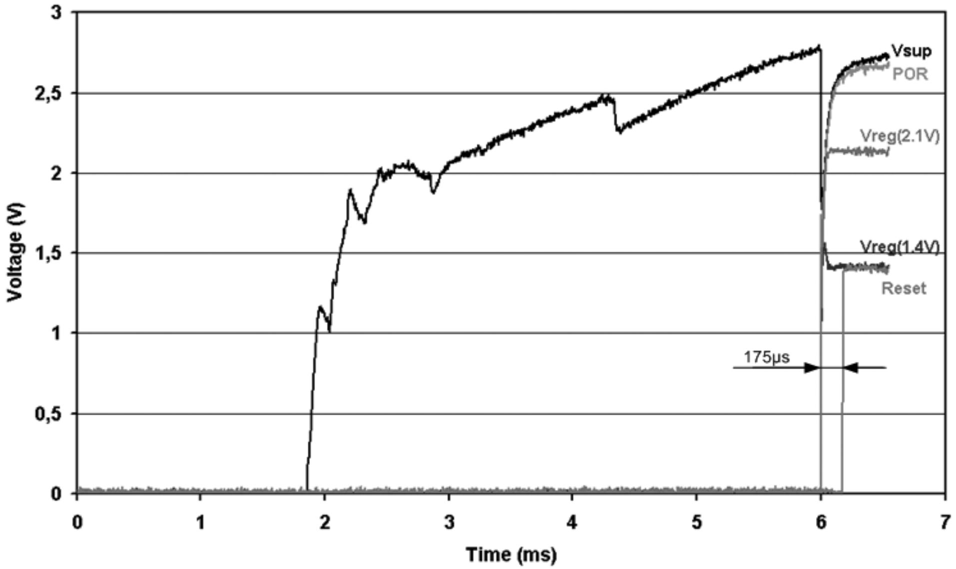
- Continuous 2W RF power emission.
- Sensor and digital core replaced by a continuous current consumption through a load resistance, supplied by an external LDO.
- Maximum distance vs. current available (I_{OUT}) analysis: of 15µA@2.5V a 2.4m.



Results
Front-end and digital core results

ASK (top) and LM (bottom) signals.





Start-up measurement of the analog front-end.

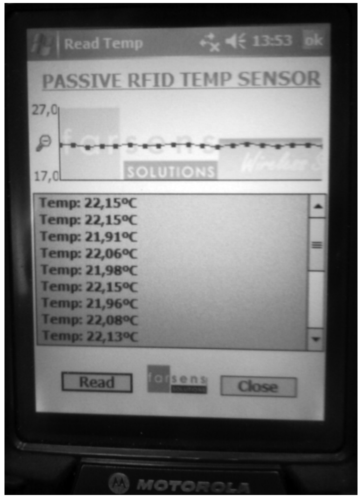
FE consumption: 7.4µA

FE input impedance: 7.8Ω + j47.7Ω

FE load modulator phase-shift: 85°

Results

System results (I)



Read Temp 13:53 ok

PASSIVE RFID TEMP SENSOR

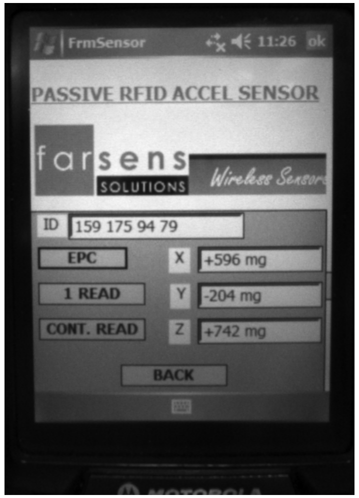
27,0

17,0

Temp: 22,15ºC
Temp: 22,15ºC
Temp: 21,91ºC
Temp: 22,06ºC
Temp: 21,98ºC
Temp: 22,15ºC
Temp: 21,96ºC
Temp: 22,08ºC
Temp: 22,13ºC

Read Close

Wireless temperature monitoring



FrmSensor 11:26 ok

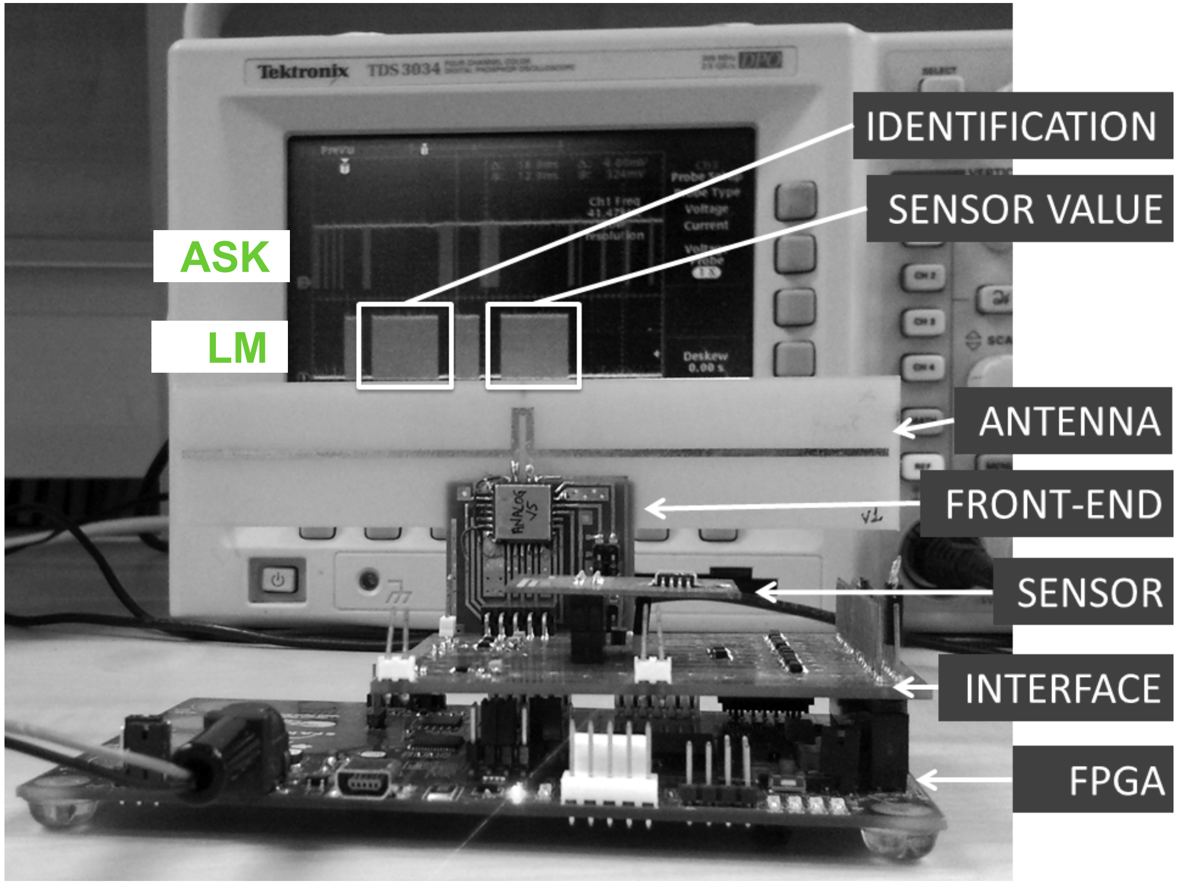
PASSIVE RFID ACCEL SENSOR

ID 159 175 94 79

EPC	X	+596 mg
1 READ	Y	-204 mg
CONT. READ	Z	+742 mg

BACK

Wireless Acceleration monitoring



Results
System results (II)

- Wireless temperature sensor and a wireless accelerometer.
  - Monitoring the temperature of the tag up to a distance of 2m.
  - Monitoring the 3-Axis accelerometer of the tag up to a distance around 1m.
- Operation distance limitations: MOTOROLA hand-held MC9090 at 30dBm.
  - Reduced output power of the hand-held commercial readers.
    - Limitation of 3dB if compared with the previous analysis
  - Not continuous emissions.
    - The APIs provided by the vendor there is no possibility to have a continuous RF emission without sending commands.

Conclusions

- In order to maximize the communication range of a passive RFID sensor, the analog and digital core of the tag have been optimized with a deep analysis of the dynamic power consumption.
- Measured results show a successful wireless communication from a 2W EIRP output power reader to a digital module plus low power sensor (temperature, pressure, humidity, etc.) with average power consumption lower than 37.5µW.
- The design and experimental results of a battery-less RFID sensor device compatible with the EPC C1G2 protocol has been presented as a suitable solution for many applications.
- These characteristics allow the use of the proposed sensory system in a battery-less wireless sensor network.
- Many advances in low power analog and digital designs must be done to impact in healthcare devices, where miniaturization and cost are mandatory.

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