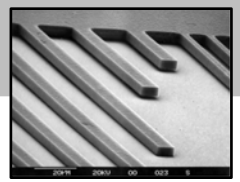
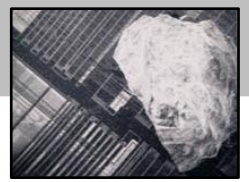
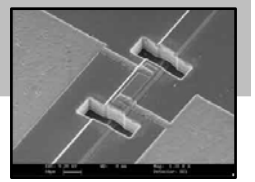
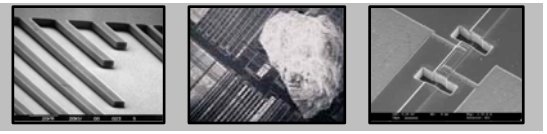
University of Pavia
Integrated Microsystems Laboratory

Low power analog electronics for portable and autonomous applications

Franco Maloberti

franco.maloberti@unipv.it



OUTLINE

- Introduction
- Challenges of State-of-the-art Technologies
- Analog Power-aware Design
- Design examples
- Digital Assisted Analog
- Conclusions

Introduction

RATIONALE

- In the fast growing electronic world, analog integrated circuits continue playing an important role for sensing and networking, security and safety, healthcare medical and life science.
- Two important and essential features of many modern systems are connectivity and portability.
- Low power, or better micro-power design is very important because having a long battery life or even ensuring battery-less operation are essential features. The reduction of the supply voltage is not imposed by just an evolving IC technology but also by the need of minimum power consumption.
- Therefore, low-voltage analog and A/D design is an important research topic.

Research for portable and autonomous needs

Technology advancements and the electronics market evolution more and more favor applications with nomadic features:

- Limited power refueling;
- Autonomous operation (no power specifically provided with capability to acquire the power that needs and modulate its activity depending on the available power budget).

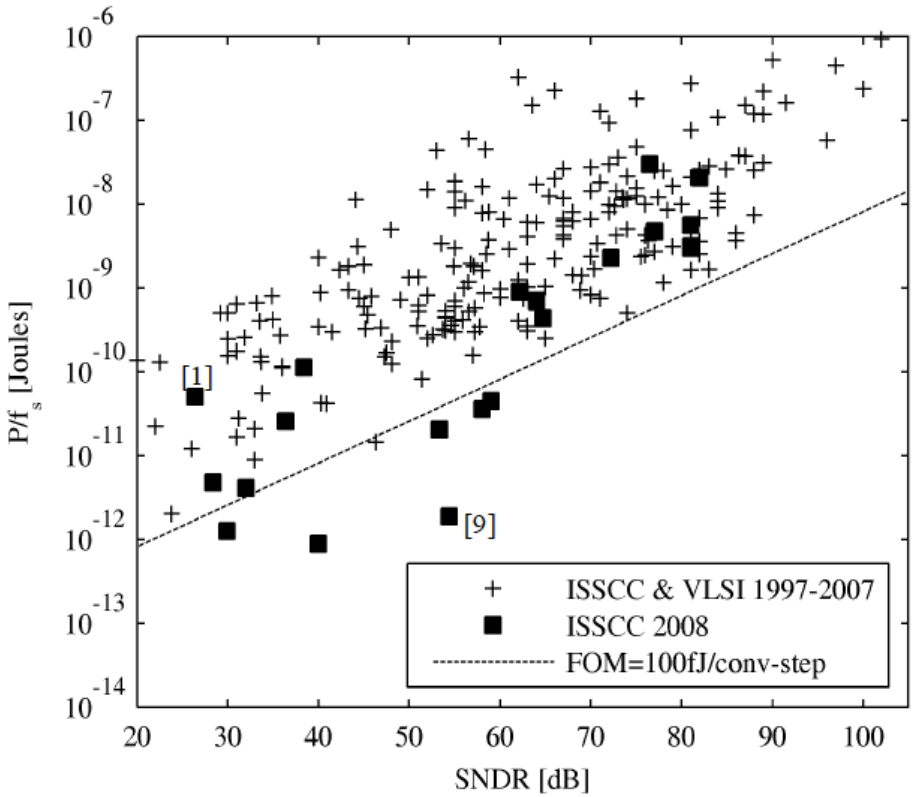
Nomadic electronics impose an optimum trade-off between power and performance $\Rightarrow$ Minimum power and its aware use.

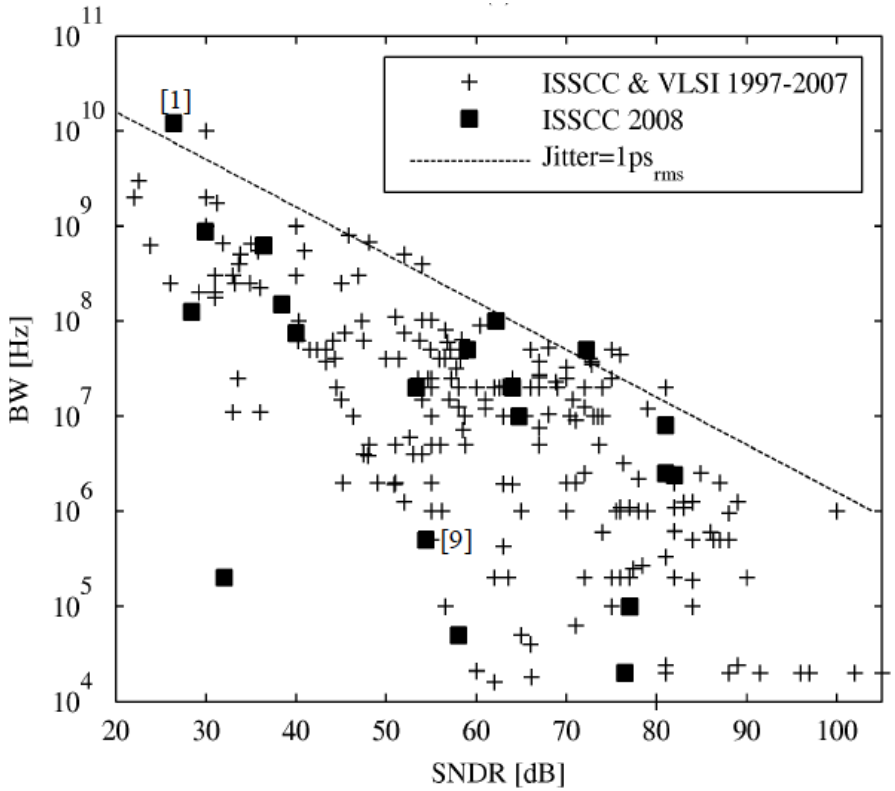
Hot Topics

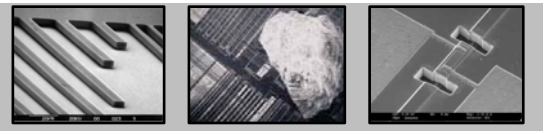
- Ultra-low power analog conditioning;
- Ultra-low power data conversion;
- Power aware digital design;
- Re-design of basic digital cells and power optimization of algorithms.
- Portable Power Management.

HOW TO MEASURE THE POWER EFFECTIVENESS?

$$FOM = \frac{P}{f_s \cdot 2^{ENOB}} \qquad ENOB = \frac{SNDR(dB) - 1.76}{6.02}$$



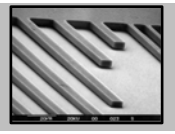
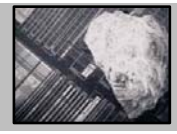
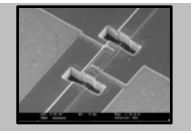




OUTLINE

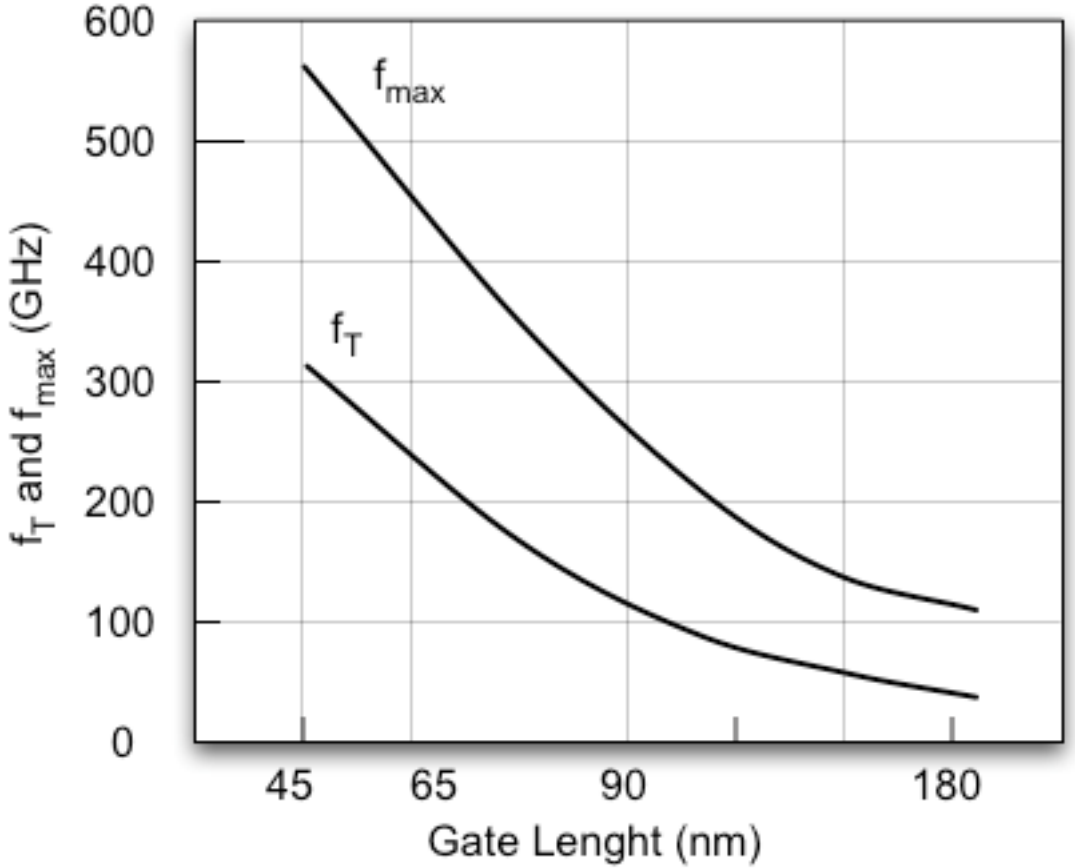
- Introduction
- Challenges of State-of-the-art Technologies
- Analog Power-aware Design
- Design examples
- Digital Assisted Analog
- Conclusions

Good and Bad of Technology

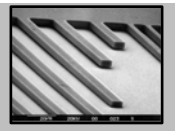
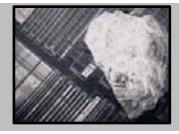
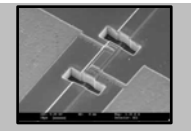




- Increase of speed → process f_T of CMOS

$$f_T \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \sim \frac{1}{L_g^2}.$$



Parameters of DSM Transistors

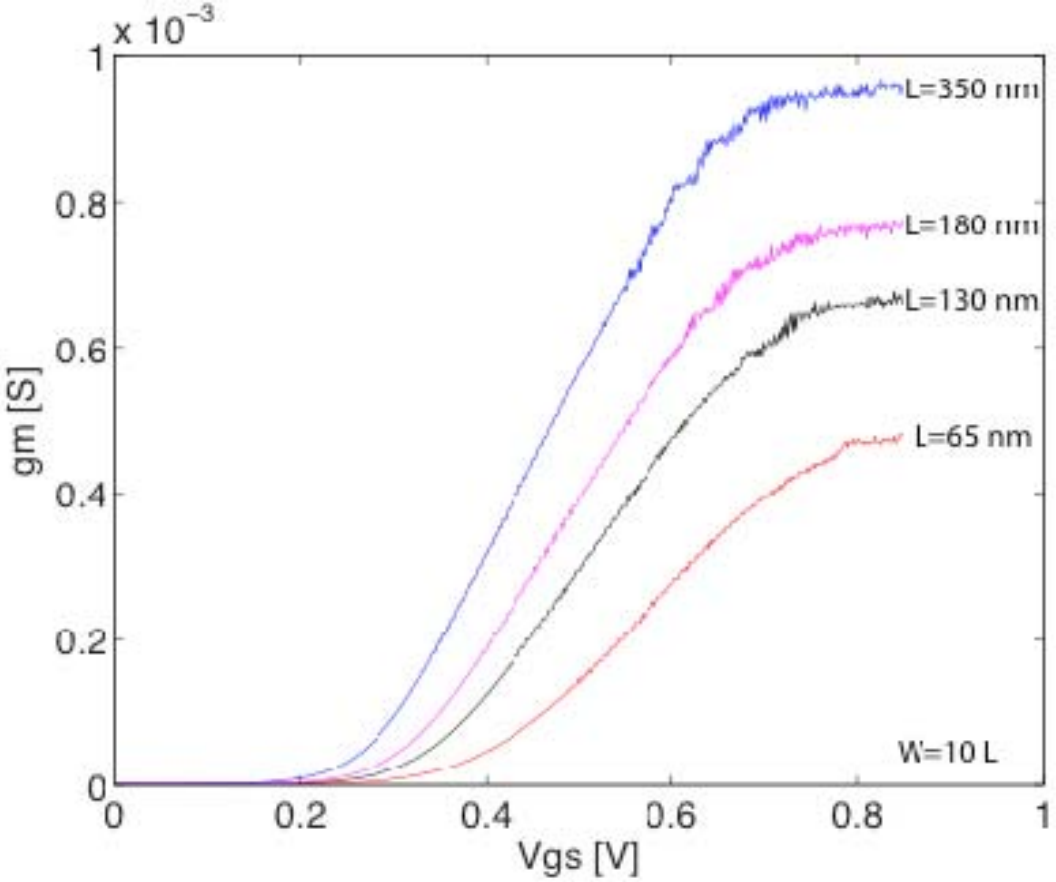




- Transconductance at saturated carrier velocity

$$I_D = (\alpha W C_{ox} V_{ov}) v_{sat} \qquad g_m = \alpha W C_{ox} v_{sat}$$

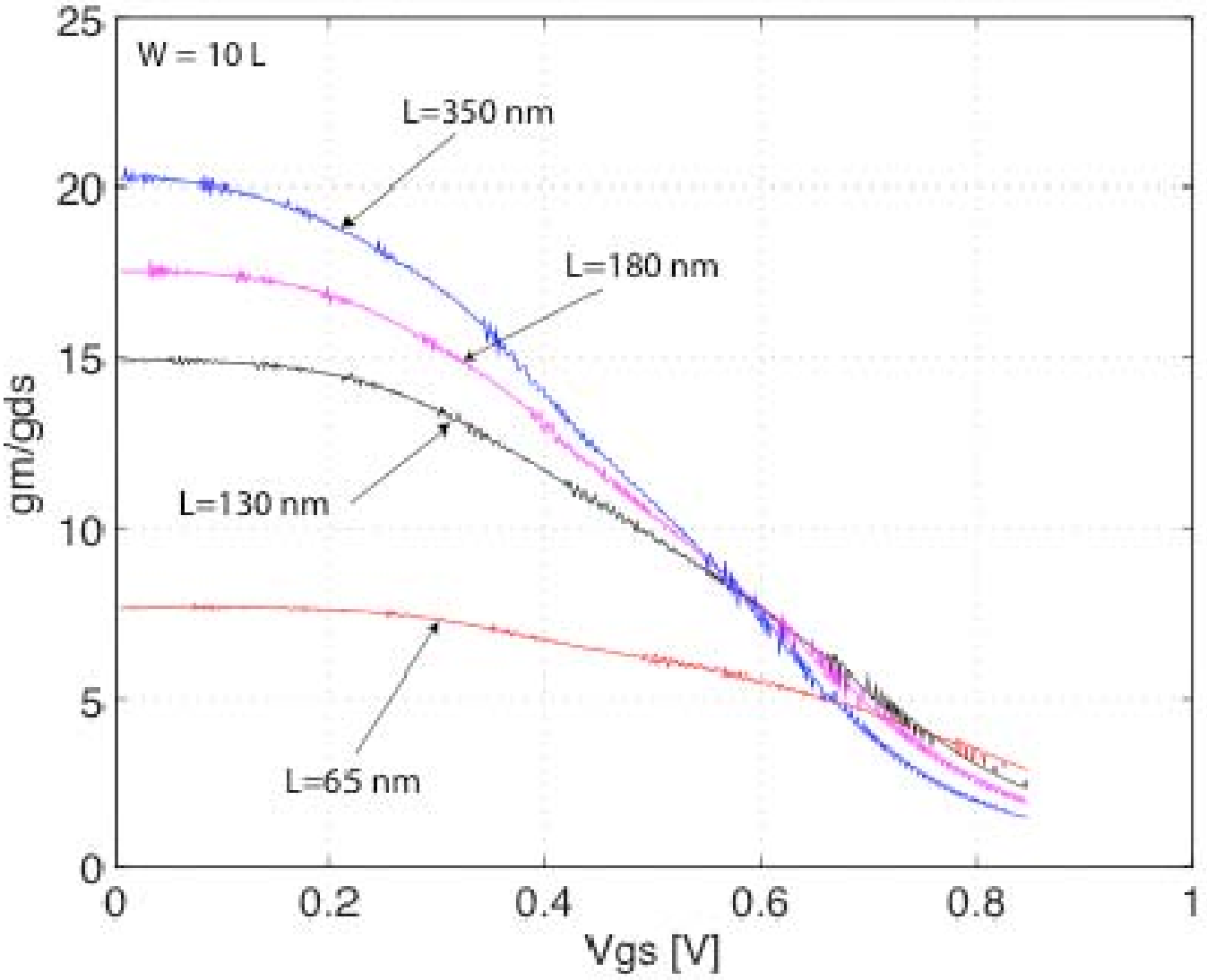
Increase the width and/or enlarge the transistor

With a 65 nm technology



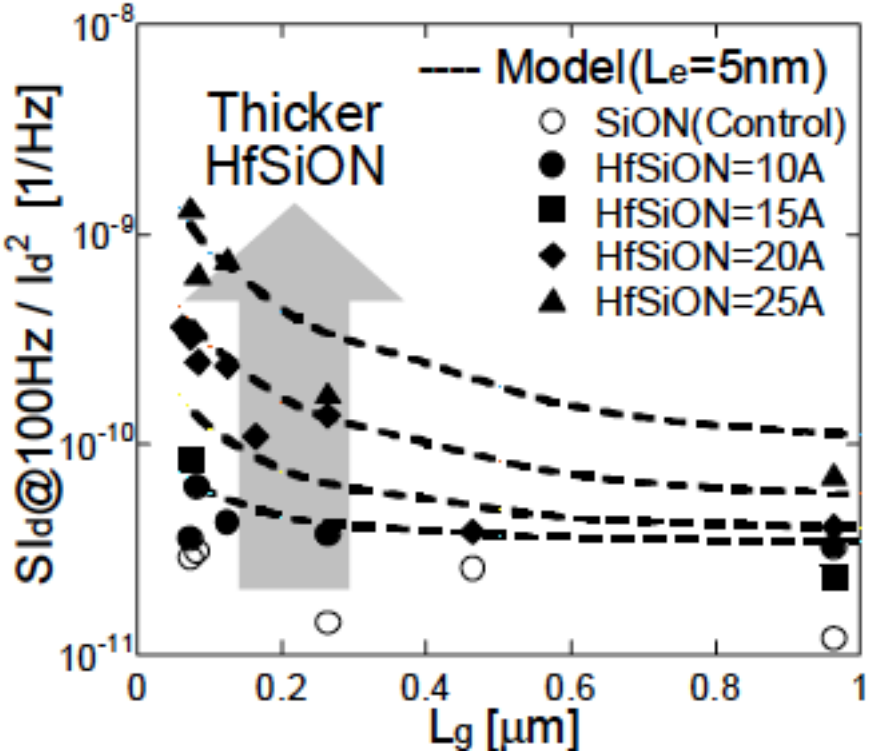
Parameters of DSM Transistors

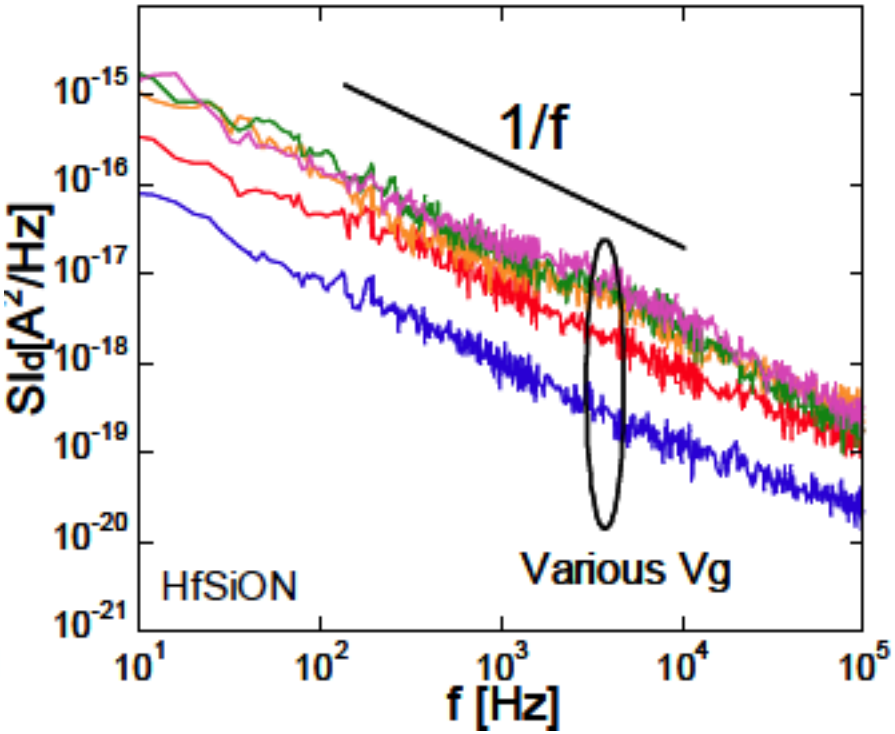
- Intrinsic gain



Parameters of DSM Transistors

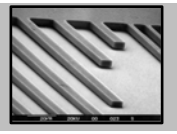
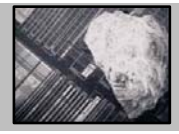
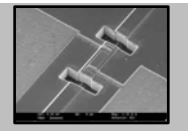
- Use of high-k oxides causes much more 1/f





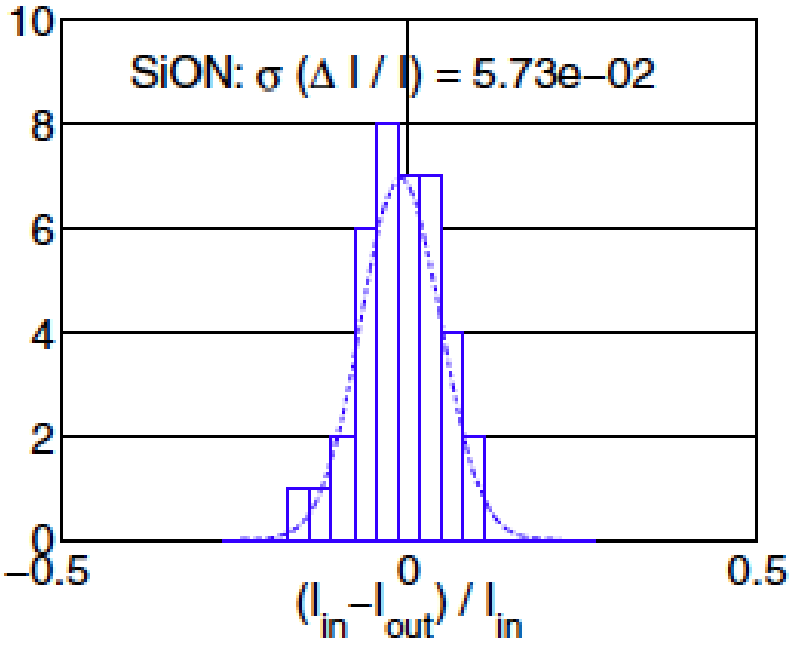
Yuri Yasuda et al.
2006 Symposium on VLSI Technology

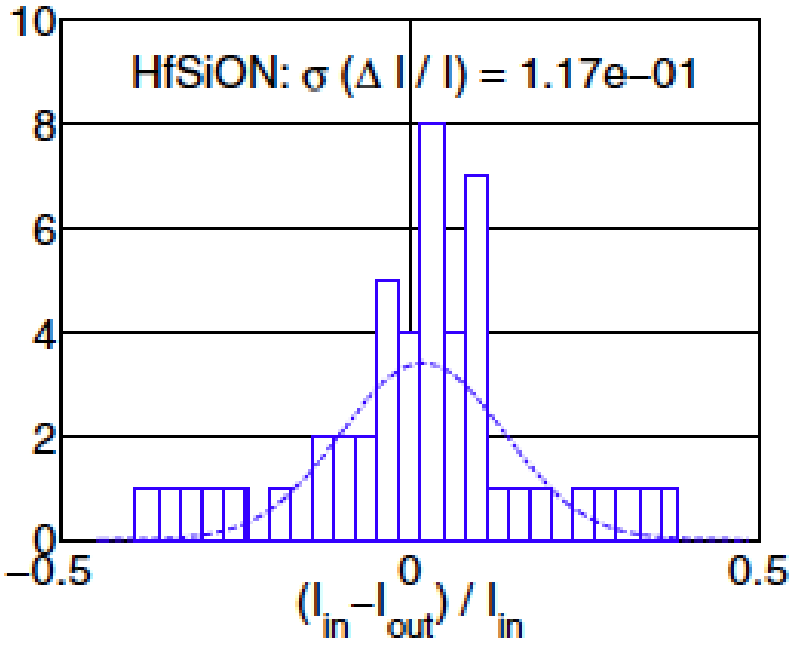
Parameters of DSM Transistors

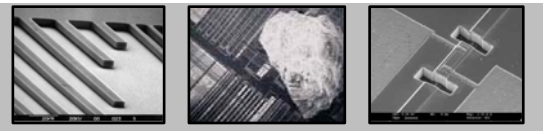
- Matching

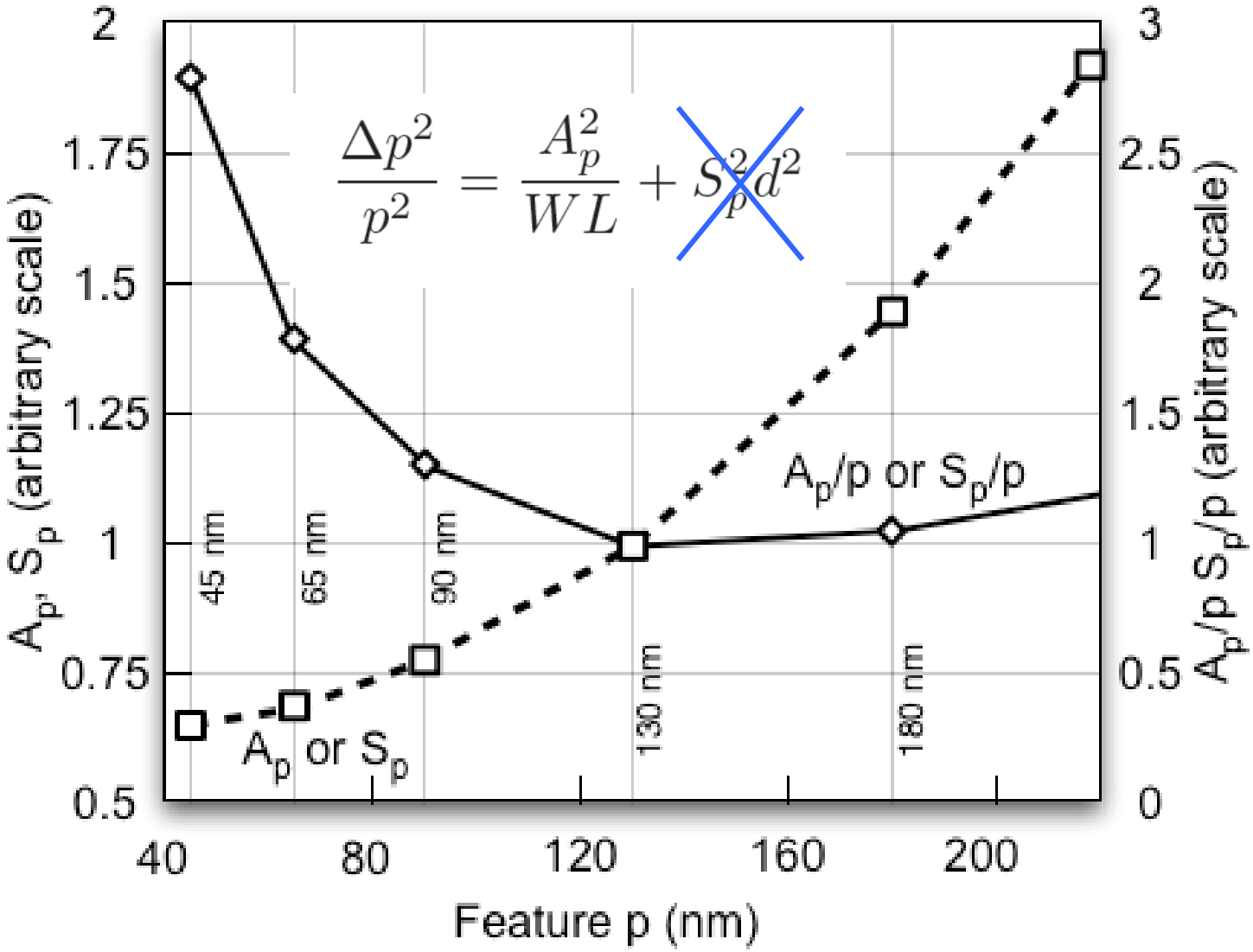
$$\frac{\Delta p^2}{p^2} = \frac{A_p^2}{WL} + S_p^2 d^2$$





Matching Parameter and Matching





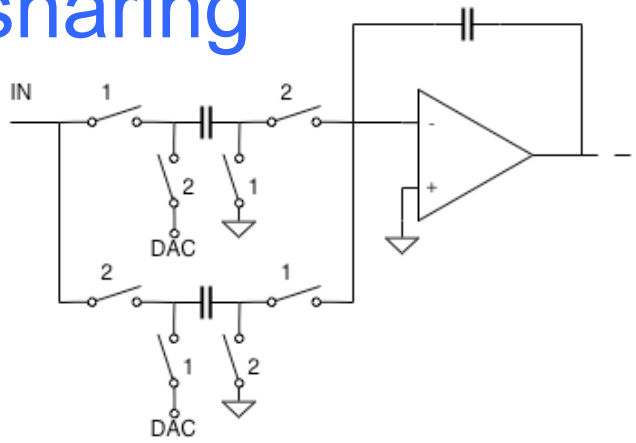
OUTLINE

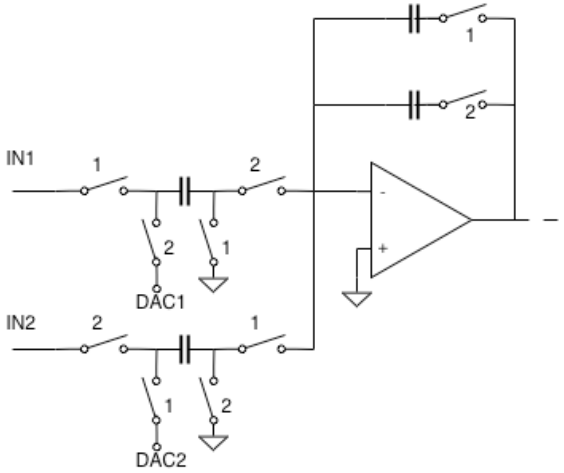
- Introduction
- Managing the power budget
- Challenges of State-of-the-art Technologies
- **Analog Power-aware Design**
- Design examples
- Digital Assisted Analog
- Conclusions

DESIGN STRATEGIES

Double sampling or Op-amp sharing

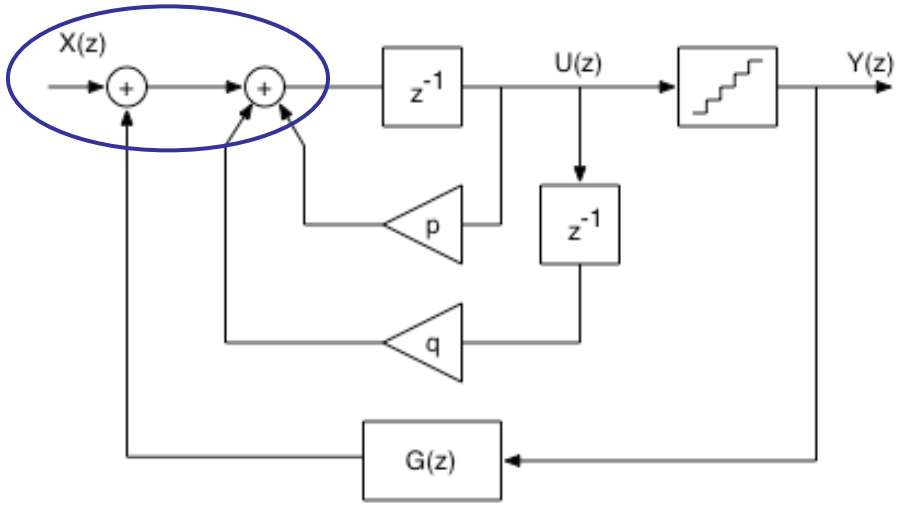
- Bandwidth of the Op-amp must be a bit higher
- No time for the virtual ground settling
- Feedback factor can be time variant
- Power saving is about 0.3 $P_{op\text{-}amp}$





Use less Op-amp than the order ΣΔ

More details and
Experimental results
J.Ko et al.
@ ISSCC 05



p = 2
q = -1
G= $2-z^{-1}$

Patent by
J.Koh @ TI

- The adding node requires using one op-amp
- The integration block is $1/(1-2z^{-1}+z^{-2})=1/(1-z^{-1})^2$
- The NTF is $(1-z^{-1})^2$
- Mismatch in capacitances moves the NTF zeros
- Solution suitable for medium resolution and low OSR

More bit or higher OSR in ΣΔ architectures

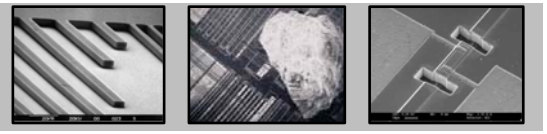
- Multi-bit helps in reducing the power consumption:
  - Second order -> double the clock to get 2.5 extra bit
    - Doubling the clock means more than doubling the power
    - 2.5 bit means $2^{2.5}$x = 5.6x the number of levels used in the ADC and DAC (5.6x comparators)
- Consider a second order ΣΔ with a 2-bit DAC
    - $P_{op\text{-}amp}$=1 mW; P_{comp}= 30 μW
    - $P_{\Sigma\Delta}$=2· $P_{op\text{-}amp}$ + (2^2-1)· P_{comp} + P_{dig}≈ 2 +0.09+0.1=2.2 mW
  - Doubling the clock frequency
    - $P_{op\text{-}amp}$=2 mW; P_{comp}= 40 μW; $P_{\Sigma\Delta}$= 4.25 mW
  - Using 5.6x comparators (4.5-bit) (and a bit more digital)
    - $P_{\Sigma\Delta}$=2· $P_{op\text{-}amp}$+ 22· P_{comp}+ P_{dig}≈ 2+0.66+0.15 = 2.8 mW

Design of suitable building blocks

- The use of well established scheme can be non-optimal
  - Op-amps linearity and gain really necessary?
  - Existing comparator architecture are optimal?
  - Can we trade speed with accuracy even at the block level?
- Look at the reference generator power needs
- Use of digital methods to relax the block specs

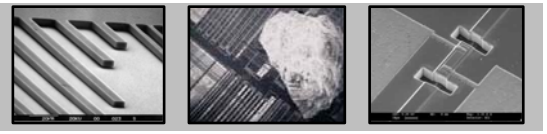
OUTLINE

- Introduction
- Managing the power budget
- Challenges of State-of-the-art Technologies
- Analog Power-aware Design
- Design examples
- Digital Assisted Analog
- Conclusions



Examples

- Low-power SAR Design
- Low-power ultra-low offset op-amp



Low-power SAR Design

- Use of time-domain comparator

Low-Power SAR

LOW power is the most relevant design concern for battery-powered mobile applications.

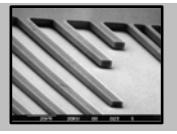
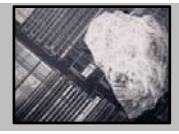
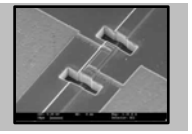
Since the ADCs operate at 10s of MS/s with 10b to 12b, the pipeline ADC is the commonly used architecture because of its power efficiency.

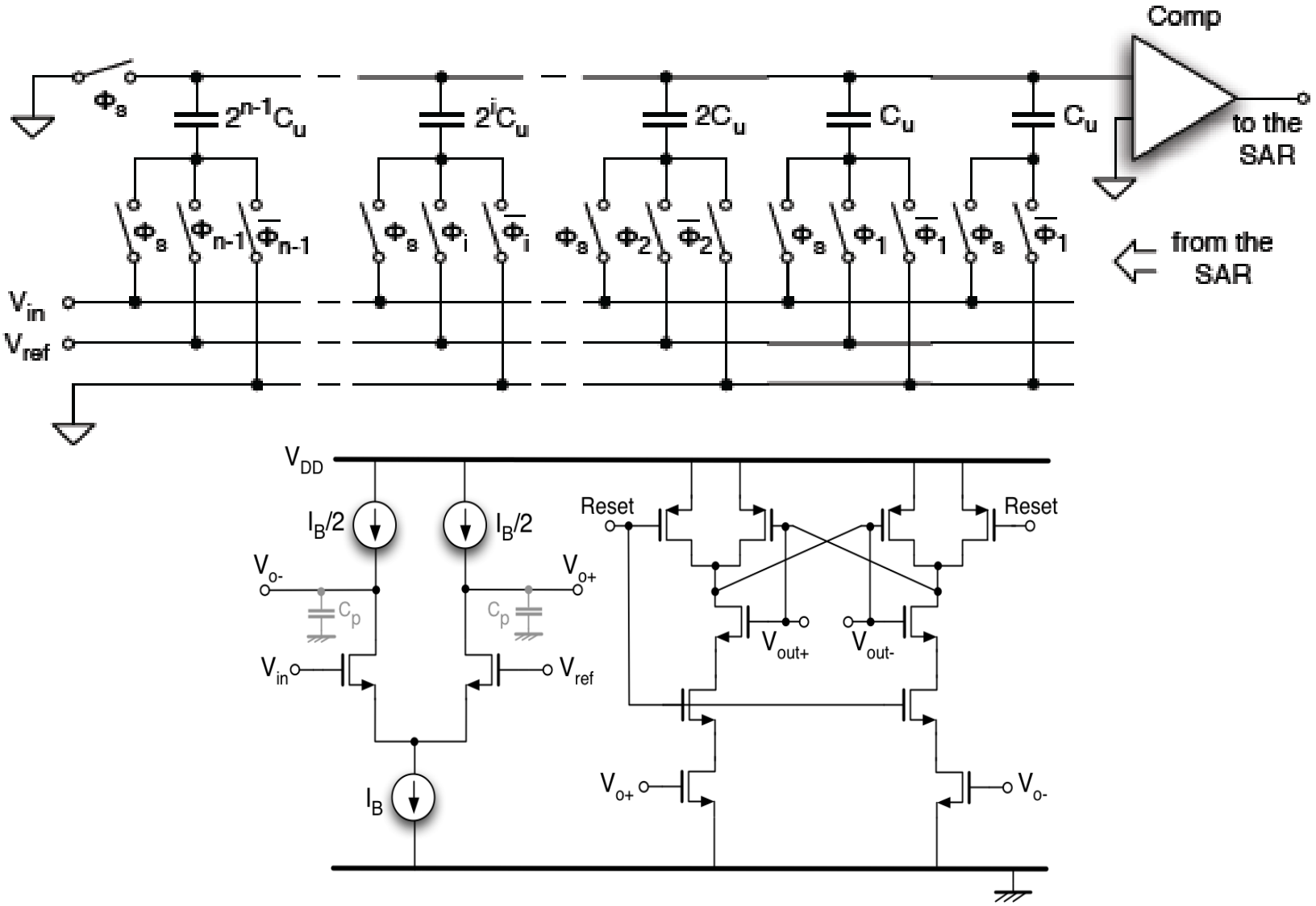
Recently, the successive approximation resistor (SAR) architecture has re-emerged as a valuable alternative to the pipelined solution.

The techniques used for low speed can be re-used for high speed.

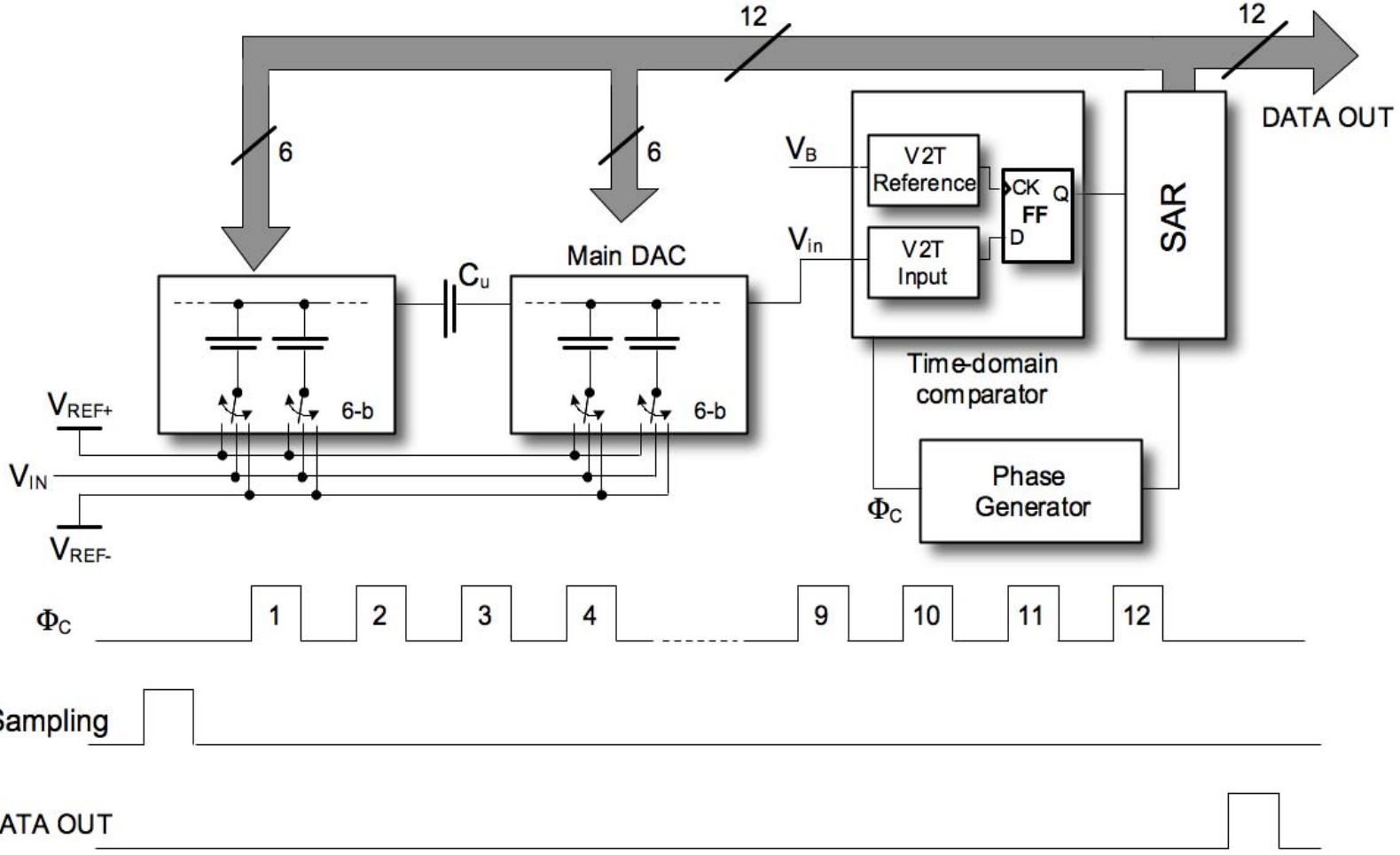
This example is a state-of-the-art FOM low speed.

Low Power SAR

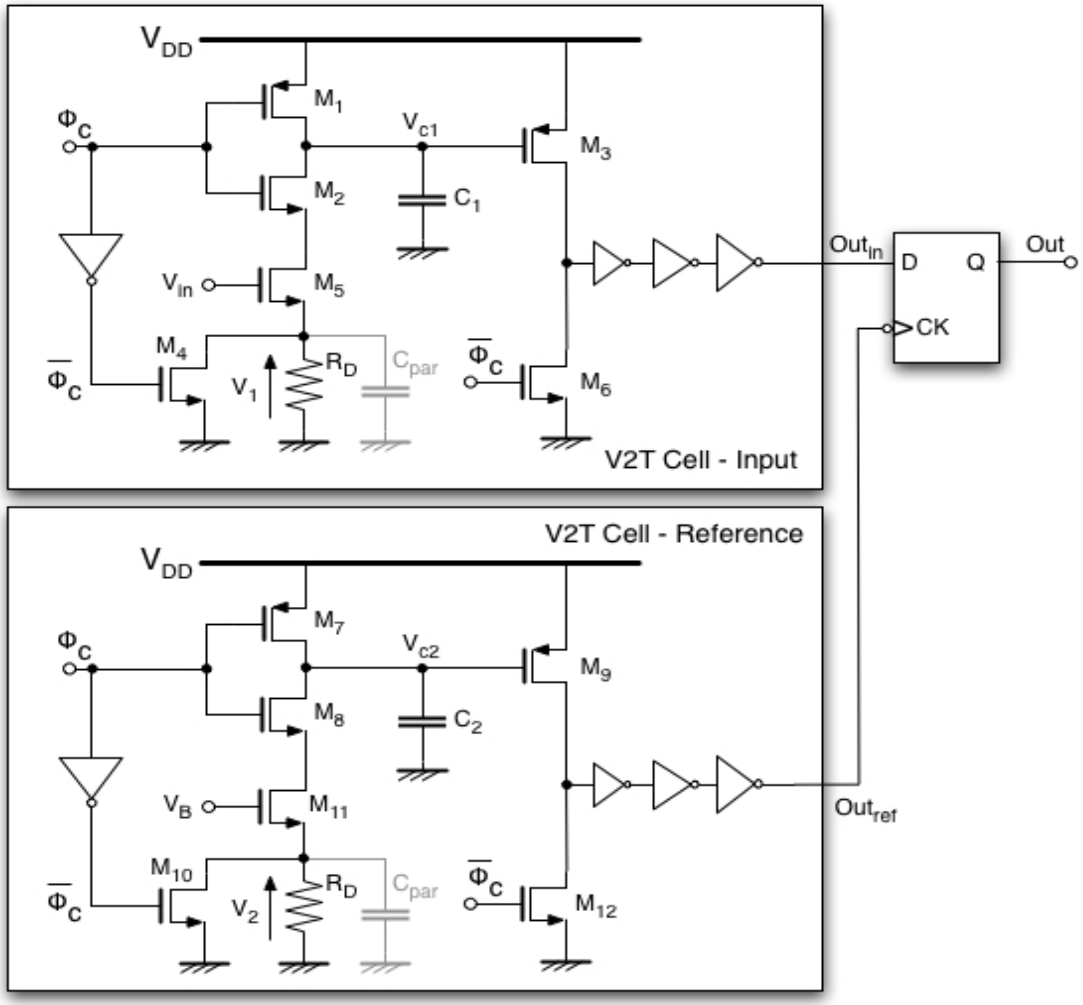


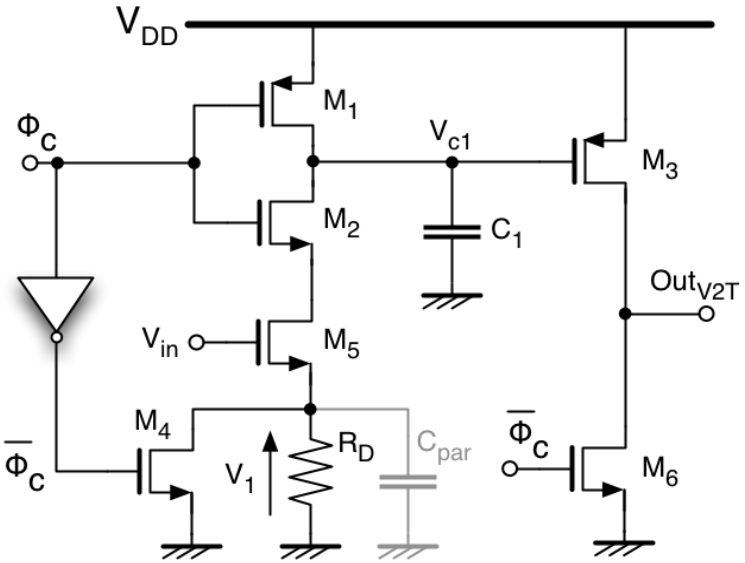
Use of unity attenuation capacitor and V2T comparator

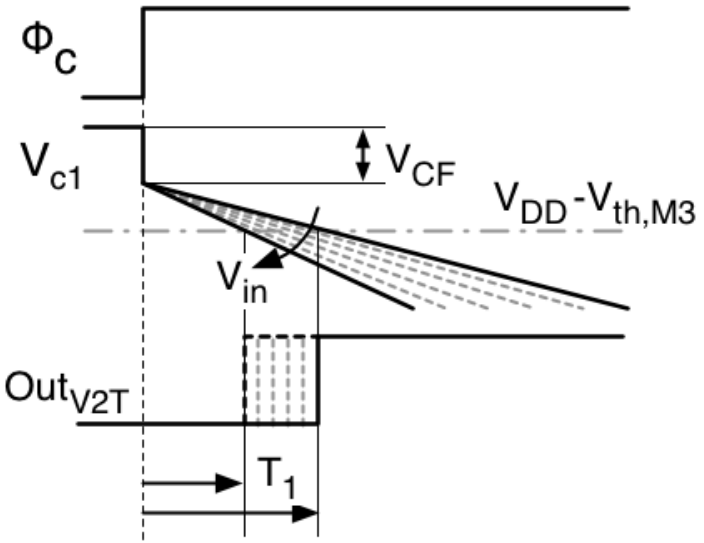


A.Agnes, E. Bonizzoni, P. Malcovati, F. Maloberti: "A 9.4-ENOB 1V 3.8µW 100kS/s SAR ADC with Time-Domain Comparator"; ISSCC 2008, pp. 246-247.

The time-domain Comparator



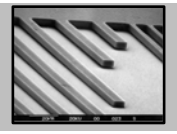
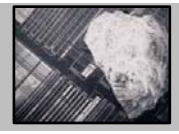
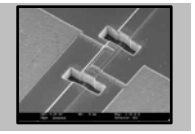




Low-Power SAR

	[3]	[4]	[5]	[6]	[7]	This Work
Technology	0.18 µm	90 nm	0.18 µm	90 nm	0.18 µm	0.18 µm
Supply Voltage	1 V	1 V	0.83 V	1 V	0.6 V	1 V
Sampling Rate	100 kS/s	20 MS/s	111 kS/s	40 MS/s	100 kS/s	100 kS/s
ENoB	10.55	7.8	7.46	8.56	8.7	9.4
ower Consumtion	25 µW	290 µW	1.16 µW	820 µW	1.3 µW	3.8 µW
FoM	167 fJ/c.-l.	65 fJ/c.-l.	60 fJ/c.-l.	54 fJ/c.-l.	31 fJ/c.-l.	56 fJ/c.-l.

Low-Power Ultra-Low Offset Op-Amp

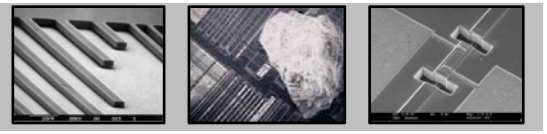
Low offset and very high gain for sensor signal amplification

Low power also important

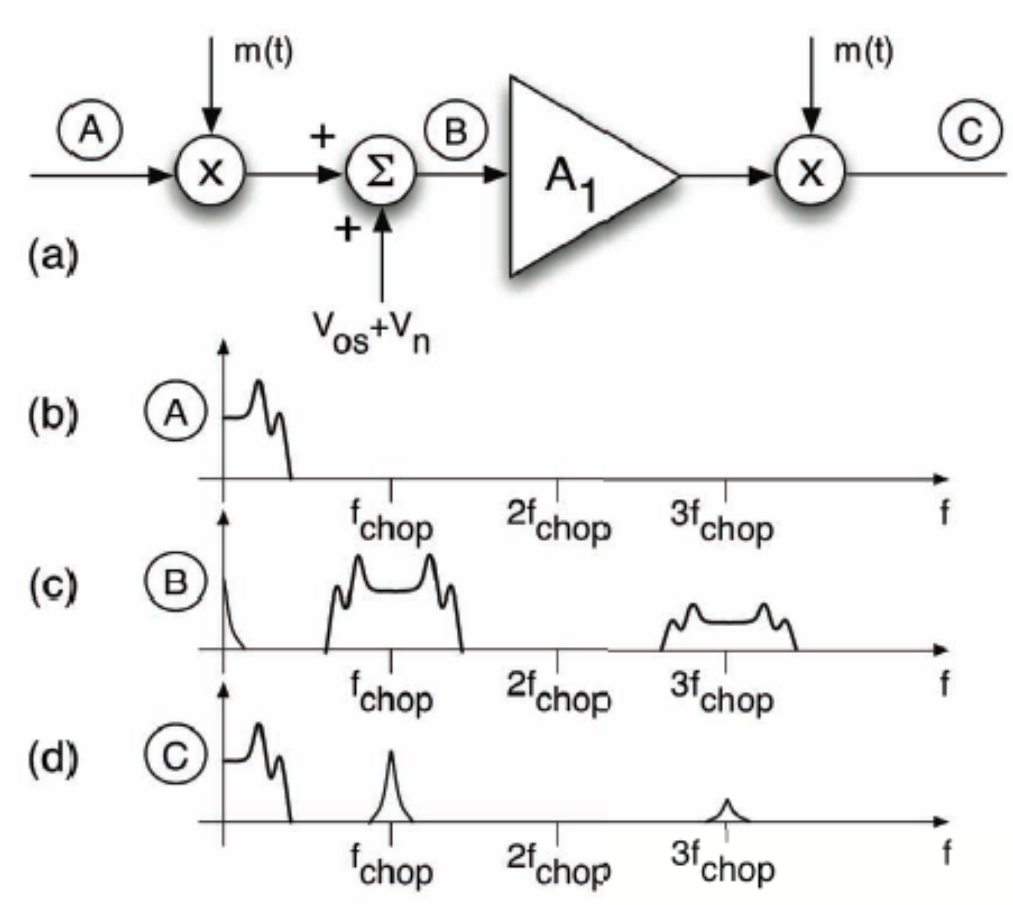
Large amplifications admit low phase margin
(we can spare power)

Conventional methods for low offset:

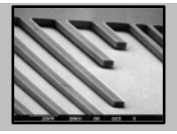
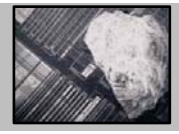
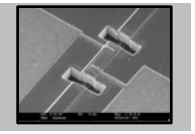
- Auto-zero
- Chopper



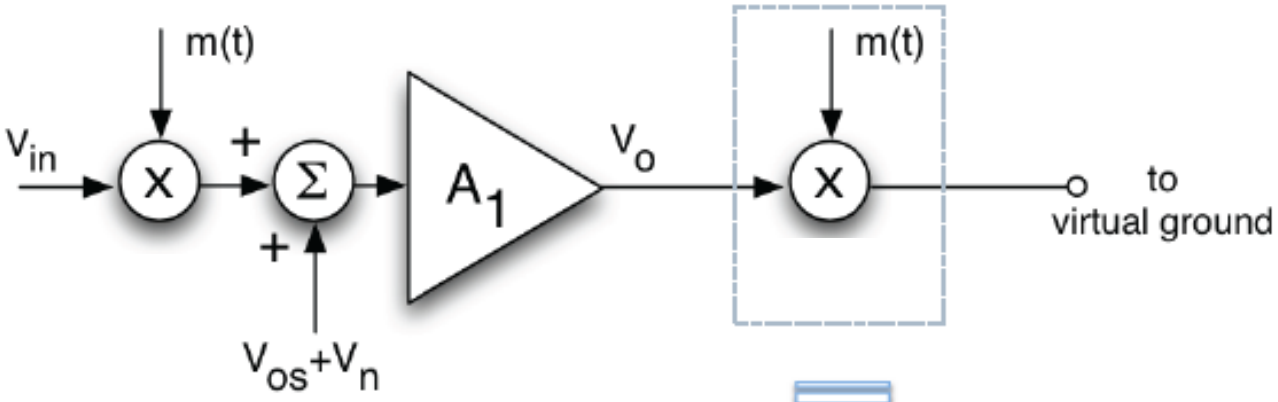
Chopper Method



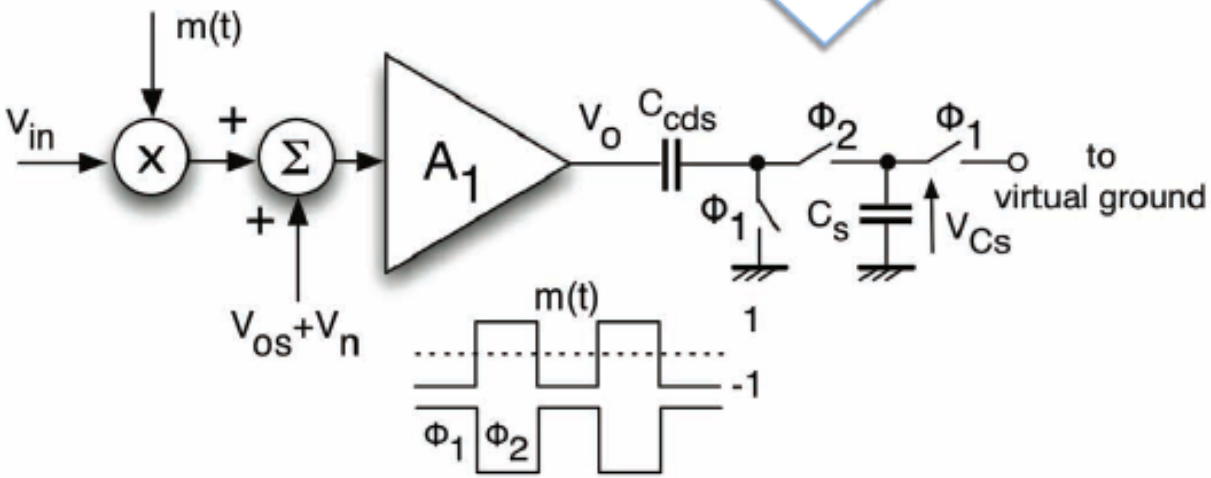
Low-Power Ultra-Low Offset Op-Amp

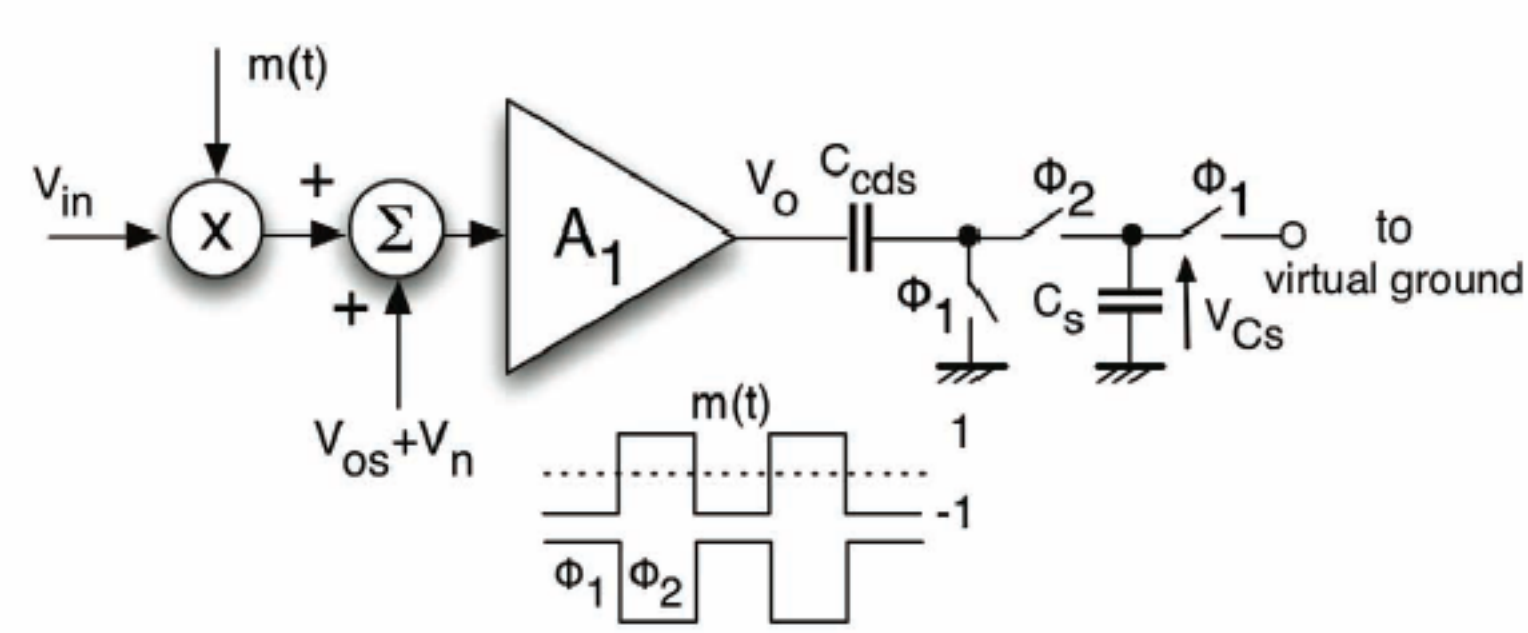




Conventional



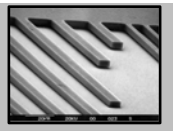
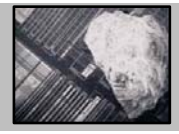
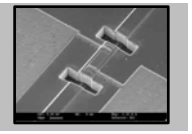
Proposed

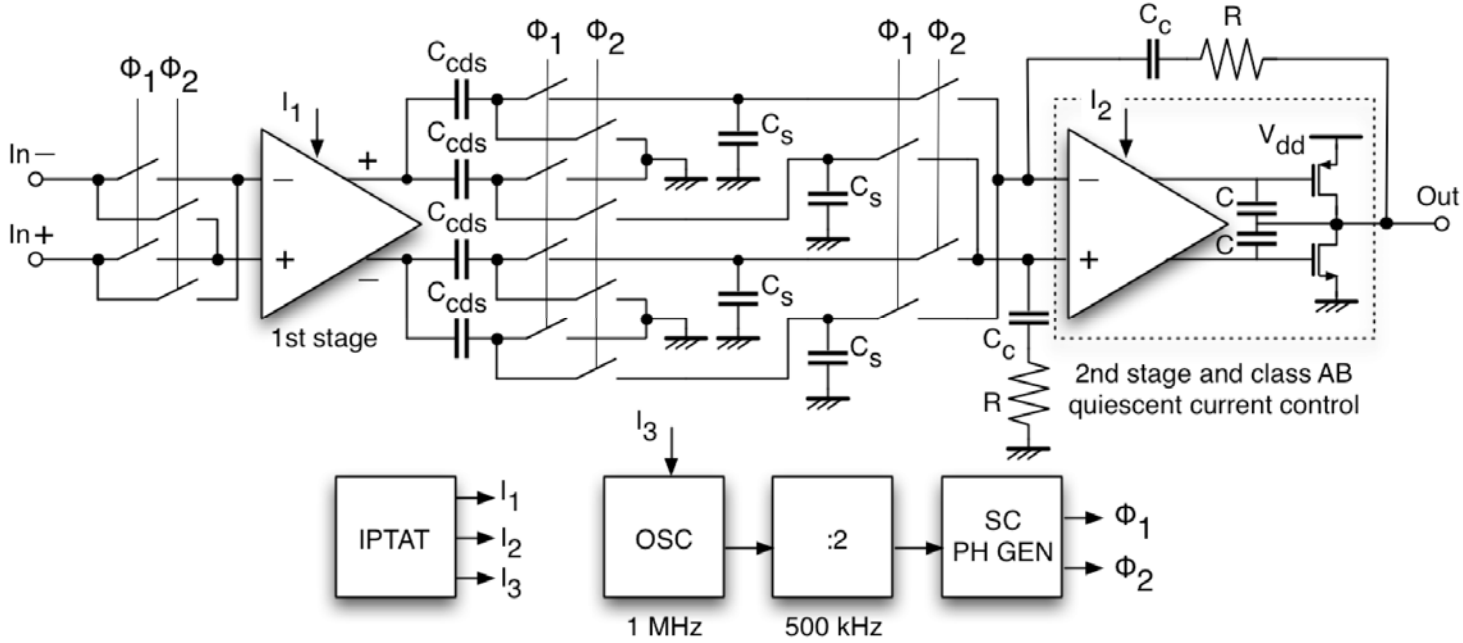




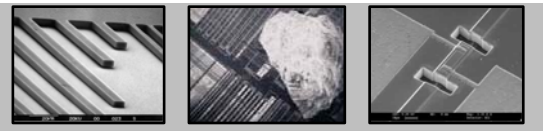
If offset and 1/f noise do not saturate the gain stage, their contribution is removed by AC coupling while the signal is detected by the correlated-double sampling scheme

Low-Power Ultra-Low Offset Op-Amp

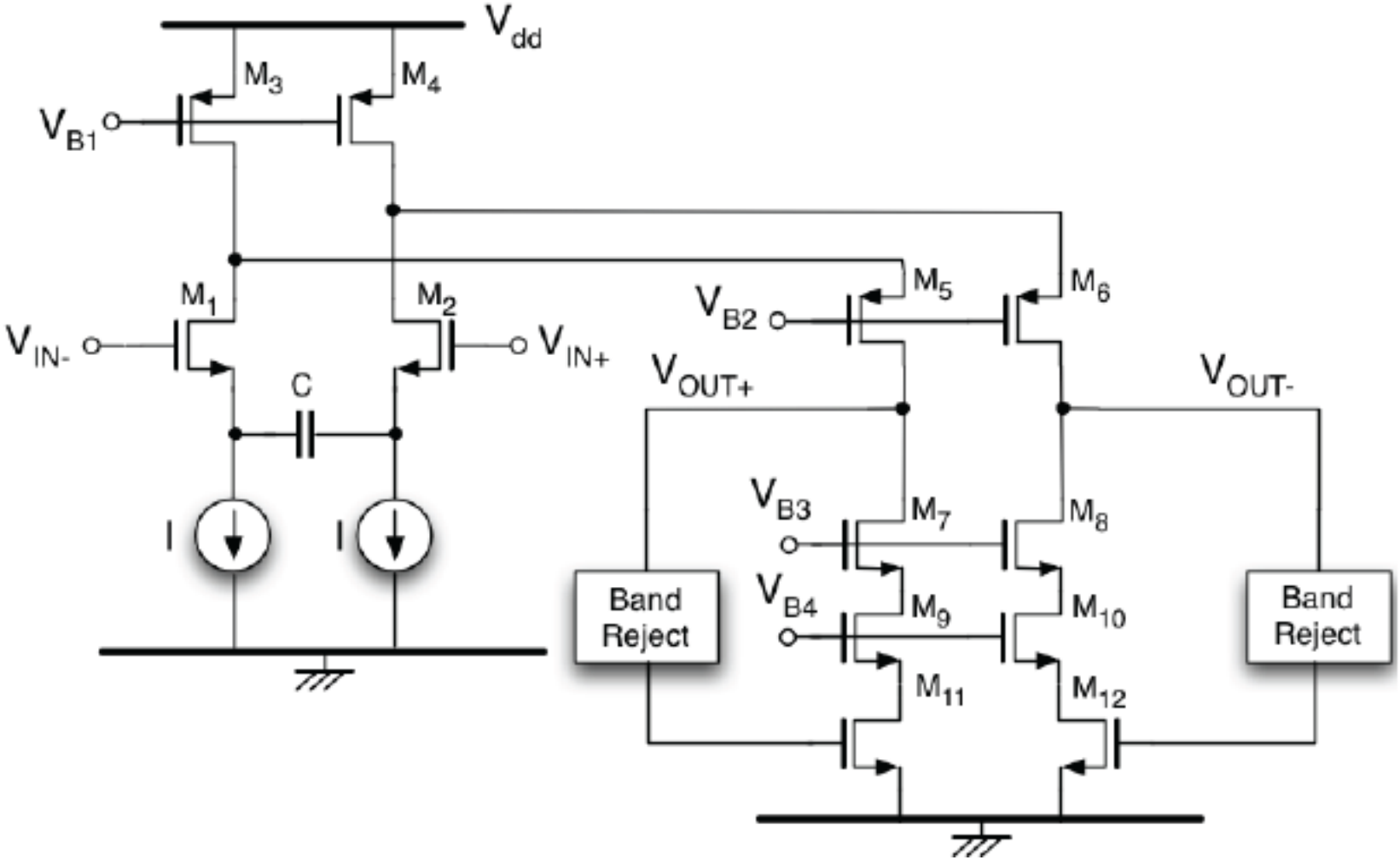




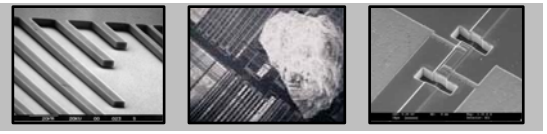


- Two CDS schemes in ping-pong fashion on both outputs
- AC coupling removes offset but open the loop at DC ➔ keep the DC output under control and well below the saturation



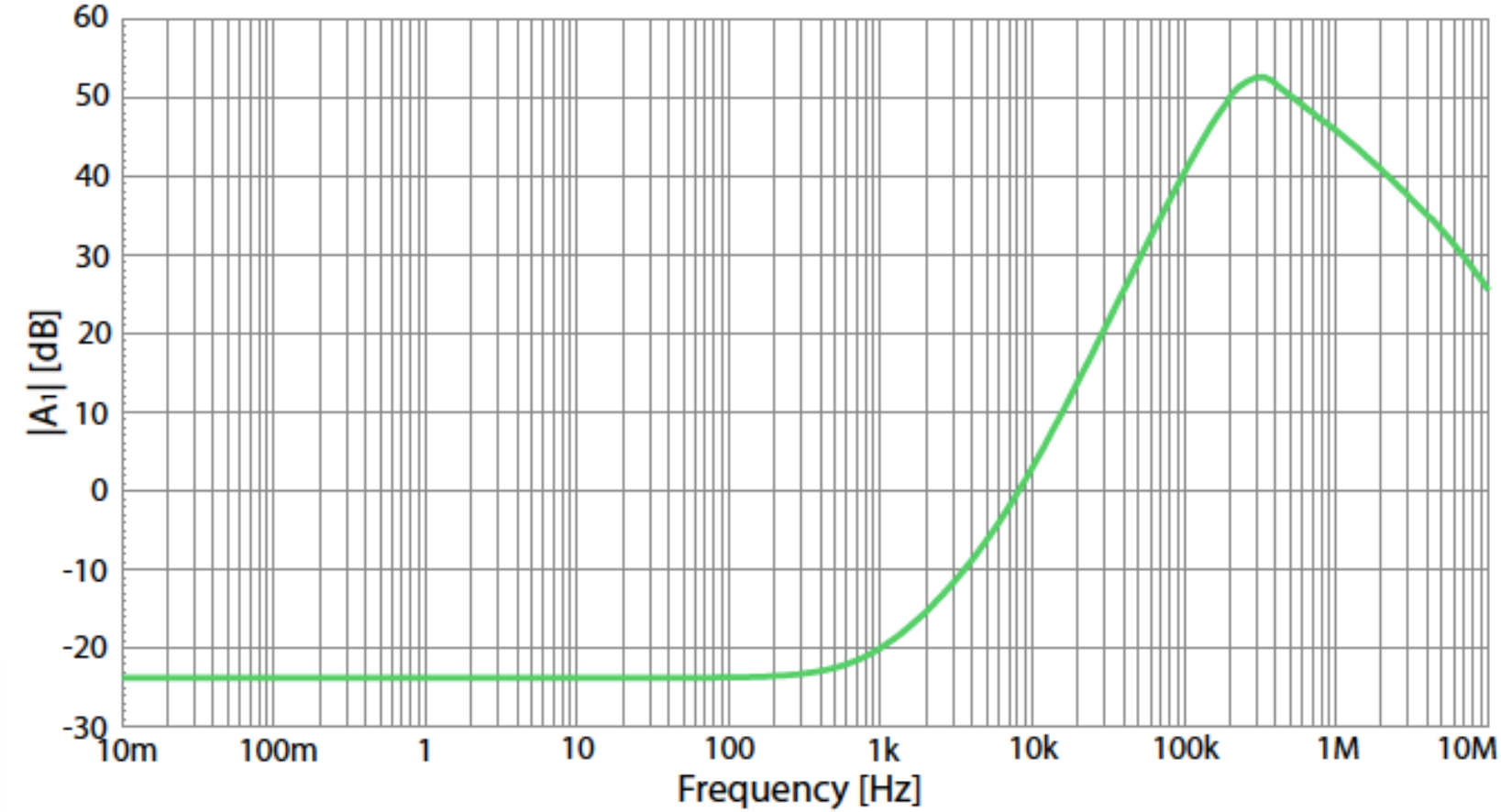
Local DC feedback ➔ Residual A_1, A_2, A_3





Transistor Level Simulation Results

Mixed 0.18-0.5 μm CMOS Technology



Low-Power Ultra-Low Offset Op-Amp

Supply Voltage	1.8 → 5V
Chopping Frequency	500 kHz
Input Noise Density at DC	37 nV/√Hz
Offset Voltage Standard Deviation	1.94 µV
Analog Supply Current	12.8 µA
Digital Supply Current	1.6 µA
Common Mode Input Range	0 → 5 V
GBW (extrapolated)	260 kHz
Offset Temperature Dependence	<0.03 µV/°C
Process	Mixed 0.18-0.5µm CMOS
Chip Area (Including Pads)	1.21 mm x 0.95 mm
Noise Efficiency Factor	5.5

OUTLINE

- Introduction
- Managing the power budget
- Challenges of State-of-the-art Technologies
- Analog Power-aware Design
- Design examples
- Digital Assisted Analog
- Conclusions

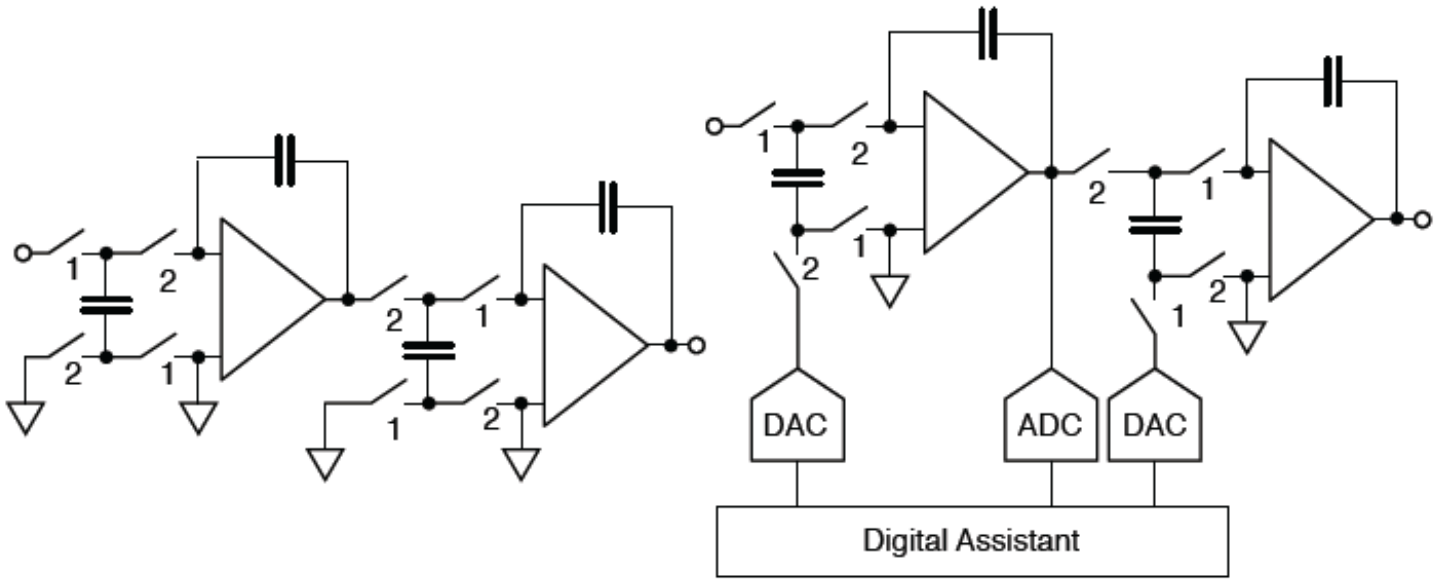
Digital Calibration

- The real advantage of thin line-width technologies is the huge number of transistors available with which we can perform complex digital functions and dynamically store huge data
- Foreground (or offline) calibration, that uses specific time-slots for calibration, and background calibration (or online), that performs the circuit calibration during the normal operation of the circuit
  - Background calibration is more complex than foreground because it requires to ensure normal operation together with calibration.
  - There are two main approaches: the use of circuit redundancy or the use of test terms added to the signal.

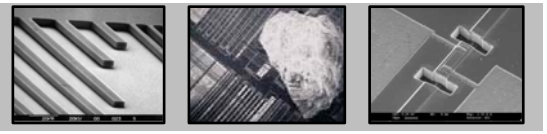
ADC Energy versus Digital Energy

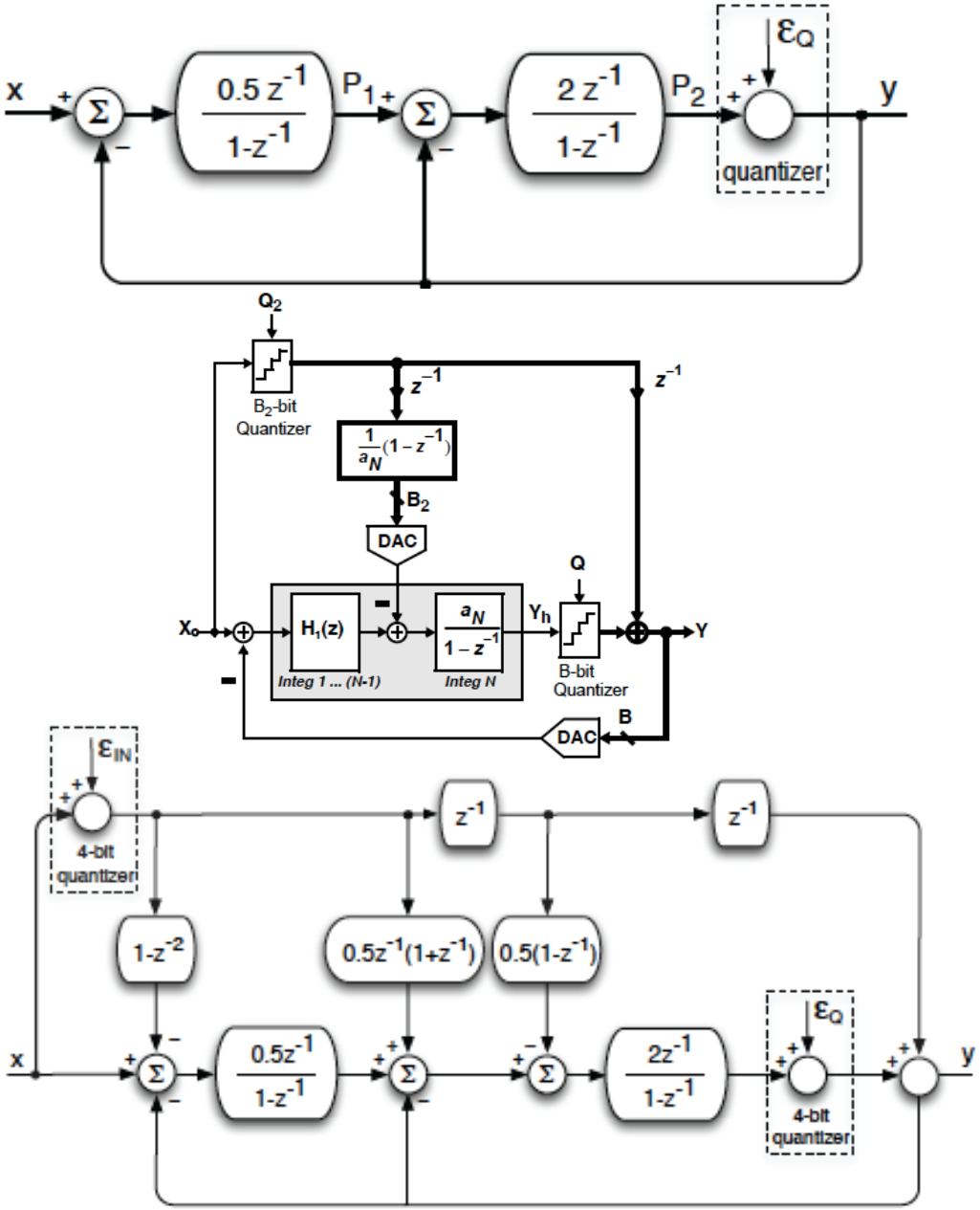
- Interesting metric to look at
  - How many digital gates can you toggle for the energy needed in one A/D conversion?
- Example
  - Standard digital gates (NAND2) in 0.13mm CMOS consume about 6nW/Gate/MHz
    - Energy/Gate = 6fJ
  - State-of-the-art 10-bit ADC consumes 0.1mW/MSps
    - Energy/Conversion = 0.1nJ
  - Energy equivalent number of gates
    - 16.7K

- Digitally Assistant Analog
  - The digital assistant analog techniques are now in an infancy phase.
  - It is expected that the method will significant grow for helping, in addition to digital calibration, the analog designer in facing the limits of DSM technologies

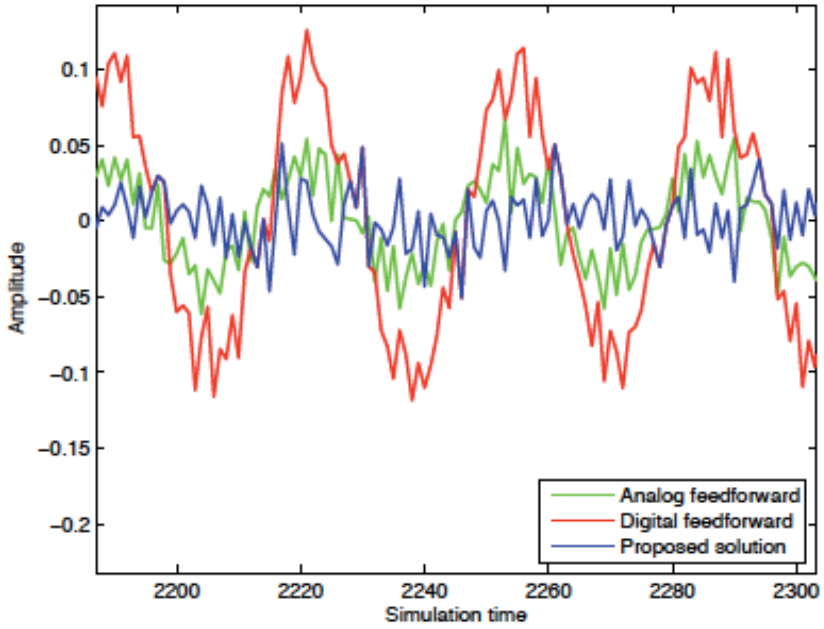


Digital Control of Analog Circuits



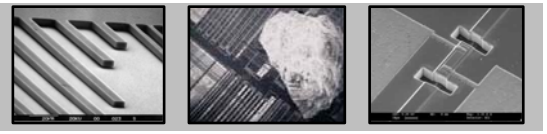


Use of digital representations of signals to improve analog performances of sigma-delta modulators



OUTLINE

- Introduction
- Managing the power budget
- Challenges of State-of-the-art Technologies
- Analog Power-aware Design
- Design examples
- Digital Assisted Analog
- Conclusions



- Portable and autonomous applications need power efficient data converters
- Solutions involve architecture optimization, trade-off and, it may be, choice of the optimal technology
- Remember that the optimum can require extra-bit in the quantizer to compensate for power and speed needs
- Examples are just examples and not an indication of a unique path to find the optimum
- Consider more and more the advantages offered by the digital processing at zero cost.